OLED DISPLAY MODULE

Preliminary Product Specification

CUSTOMER	**Standard**	
PRODUCT NUMBER	**DD-9696FC-2A**	
CUSTOMER APPROVAL		**Date**

INTERNAL APPROVALS		
Product Mgr	Doc. Control	Electr. Eng
Bazile Peter	**Anthony Perkins**	**Luo Luo**
Date: 21/02/12	Date: 21/02/12	Date: 21/02/12

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REVISION RECORD

Rev.	Date	Page	Chapt.	Comment	ECR no.
A	21 Feb 12			First Issue	
B	01 Oct 12	9	3.3	Error on Pin 14~21 been rectified	
C	28 Nov 12	32	10	Update the part number information	
D	26 Jul 13	32	10	Update EVK board part number	

1 MAIN FEATURES

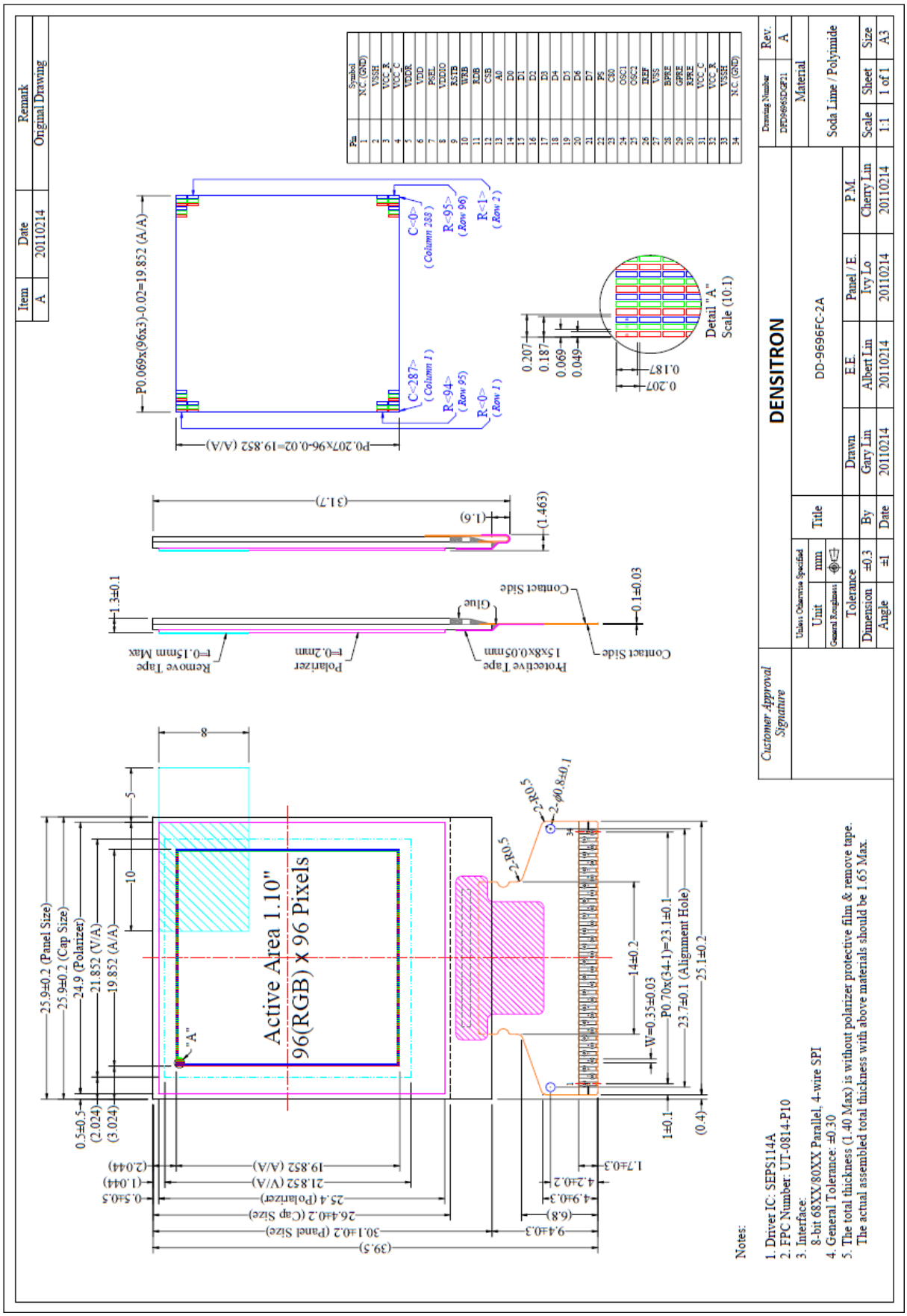
ITEM	CONTENTS
Display Format	96 x 96 Dots
Overall Dimensions	25.90 x 30.10 x 1.30 mm
Colour	65.536 Colour
Active Area	19.852 x 19.852 mm
Viewing Area	21.852 x 21.852 mm
Display Mode	Passive Matrix 1.10”
Driving Method	1/96 duty
Driver IC	SEPS114A
Operating temperature	-40 ~ +70
Storage temperature	-40 ~ +85

2 MECHANICAL SPECIFICATION

2.1 MECHANICAL CHARACTERISTICS

ITEM	CHARACTERISTIC	UNIT
Display Format	96(RGB) x 96	Dots
Overall Dimensions	25.90 x 30.10 x 1.3	mm
Viewing Area	21.852 x 21.852	mm
Active Area	19.852 x 19.852	mm
Dot Size	0.049 × 0.187	mm
Dot Pitch	0.069 × 0.207	mm
Weight	2.07	g
IC Controller/Driver	SEPS114A	

2.2 MECHANICAL DRAWING



3 ELECTRICAL SPECIFICATION

3.1 ABSOLUTE MAXIMUM RATINGS

VSS = 0 V, Ta = 25 ℃

Item	Symbol	Min	Max	Unit	Note
Supply Voltage for Operation	V_{DD}	-0.3	4	V	Note 1,2
Supply Voltage for I/O	V_{DDIO}	-0.3	4	V	
Supply Voltage for Display	Vcc_c	-0.3	15	V	
Operating Temperature	Top	-40	70	℃	Note 3
Storage Temperature	T_{STG}	-40	85	℃	Note 3
Life Time(100cd/m2)		10,000	-	hour	Note 4

Note 1: All the above voltages are on the basis of "VSS=0V".

Note 2: When this module is used beyond above absolute maximum ratings, permanent damage to the module may occur. Also for normal operations it's desirable to use this module under the conditions according to Section 3.2 "Electrical Characteristics" and section 4 "optical characteristic. If this module is used beyond these conditions the module may malfunction and the reliability could deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80 ℃.

Note 4: Vcc_c = 12.0V, Ta =25 ℃, 50% Checkerboard.
Software configuration follows Section 6.4 Initialization.
End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room is estimated by the accelerated operation at high temperature conditions.

3.2 ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Logic Voltage for Operation.	V_{DD}		2.4	2.8	3.3	V
Supply Voltage for I/O Pins	V_{DDIO}		1.65	2.8	V_{DD}	V
Supply Voltage for Display	V_{CC_C}	Note 5	11.5	12	12.5	V
High Level Input	V_{IH}		0.8x V_{DD}	-	V_{DD}	V
Low Level Input	V_{Il}		0	-	0.4	V
High Level Output	V_{OH}	I_{OH} = -0.1mA	$V_{DD-0.4}$	-		V
Low Level Output	V_{OL}	I_{OL} = -0.1mA		-	0.4	
Operating Current for V_{DD}	I_{DD}		-	1.5	3.5	mA
Operating Current for V_{CC_C}	I_{CC_C}	Note 6	-	6.4	8.0	mA
		Note 7	-	9.5	12.0	mA
		Note 8	-	16.0	20.0	mA
Sleep Mode Current for V_{DD}	IDD, SLEEP		-	3	5	µA
Sleep Mode Current for V_{CC_C}	ICC_C, SLEEP		-	1	5	µA

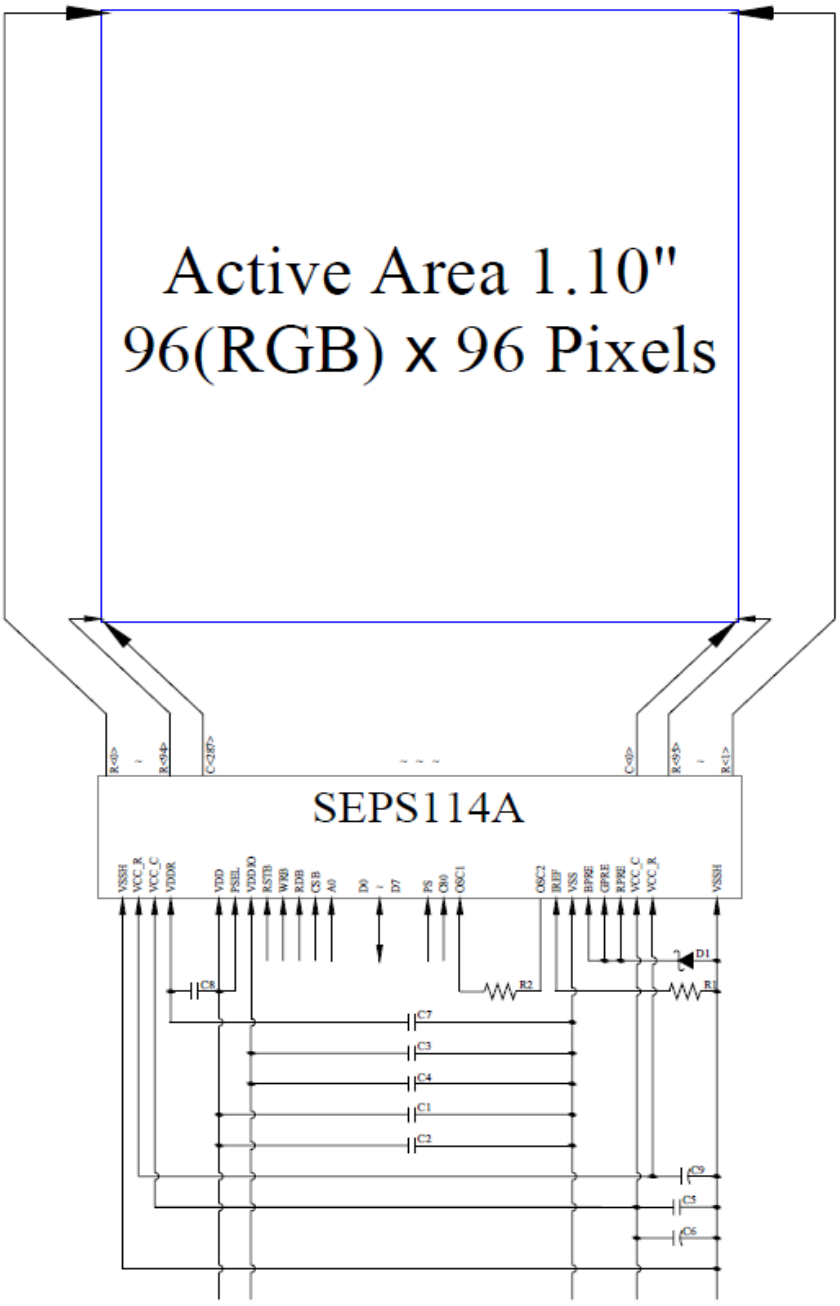
Note 5: Brightness (Lbr) and Supply Voltage for Display (V_{CC_C}) are subject to the change of the panel characteristics and the customer's request.
Note 6: V_{DD} = 2.8V, V_{CC} = 12.0V, 30% Display area turned on.
Note 7: V_{DD} = 2.8V, V_{CC} = 12.0V, 50% Display area turned on
Note 8: V_{DD} = 2.8V, V_{CC} = 12.0V, 100% Display area turned on

3.3 INTERFACE PIN ASSIGNMENT

No.	Symbol	I/O	Function
1	N.C.	-	Reserved Pin (Supporting Pin). The supporting pin can reduce the influences from stresses on the function pins. These pins must be connected to external ground as the ESD protection circuit.
2	VSSH	P	Ground of OEL Panel. This is the ground pins for analog circuits. It must be connected to external ground.
3	VCC_R	P	Voltage Output High Level for Scan Signal This is the scan driver power supply pin. A tantalum capacitor should be connected between this pin and VSS.
4	V_{CC_C}	P	Power Supply for OEL Panel This is the most positive voltage supply pin of the chip. It must be connected to external source.
5	VDDR	P	Power Supply for Core Logic Circuit This is a voltage supply pin. It can be supplied externally or regulated internally from VDD. A capacitor should be connected between this pin & VSS under all circumstances.
6	VDD	P	Power Supply for Operation This is a voltage supply pin. It must be connected to external source.
7	PSEL	I	Regulator Enable/Disable for Logic Power Supply This pin is the regulator enable/disable input of VDDR. If it is connected to VDD, the internal regulator is used. Otherwise, an external voltage supplier should be used.
8	VDDIO	P	Power Supply for I/O Pin This pin is a power supply pin of I/O buffer. It should be connected to VDD or external source. All I/O signal should have VIH reference to VDDIO. When I/O signal pins (C80, PS, D0~D7, control signals…) pull high, they should be connected to VDDIO.
9	RSTB	I	Power Reset for Controller and Driver. This pin is reset signal input. When the pin is low, initialization of the chip executed.
10	WRB	I	Read/Write Select or Write. 68XX Parallel Interface: Read (Low)/Write(High) Select 80XX Parallel Interface: Write Strobe Signal. (Active Low) While using SPI, it must be connected to Vdd or Vss
11	RDB	I	Read/Write Enable or Read. 68XX Parallel Interface: Bus Enabled Strobe (Active High) 80XX Parallel Interface: Read Strobe Signal (Active Low) While using SPI, It must be connected to Vdd or Vss.
12	CSB	I	Chip Select. Low: SEPS114A is selected and can be accessed High: SEPS11A is not selected and cannot be accessed
13	A0	I	Data/Command Control. Low: Command High: Parameter/Data
14~21	D0~D7	I/O	Host Data Input/Output Bus. These pins are 8-bit bi-directional data bus to be connected to

<table>
<tr><td></td><td></td><td></td><td>the microprocessor’s data bus.
<table>
<tr><th>PS</th><th>Description</th></tr>
<tr><td>0</td><td>D[0] SCL: Synchronous Clock Input
D[1] SDI : Serial Data Input
D[2] SDO: Serial Data Output
D[3] R/W : Serial Read(High)/Write(low)</td></tr>
<tr><td>1</td><td>8-bit Bus: D[7:0]</td></tr>
</table>
While Using SPI, the unused pins must be connected to Vss.</td></tr>
<tr><td>22</td><td>PS</td><td></td><td>Select Parallel/Serial Interface Type
Low: Serial Interface
High: Parallel Interface</td></tr>
<tr><td>23</td><td>C80</td><td>I</td><td>Select the CPU Type
Low: 80XX-Series MCU
High: 68XX-Series MCU</td></tr>
<tr><td>24
25</td><td>OSC1
OSC2</td><td>I
O</td><td>Fine Adjustment for Oscillation
The frequency is controlled by external 27kÙ resistor between OSC1 and OSC2. The oscillator signal is used for system clock generation.
When the external clock mode is selected, OSC1 is used external clock input.</td></tr>
<tr><td>26</td><td>IREF</td><td>I/O</td><td>Current Reference for Brightness Adjustment.
This is the current reference pin to generate precharge and driving current. A 39kΩ resistor should be connected between this pin and Vss.</td></tr>
<tr><td>27</td><td>VSS</td><td>P</td><td>Ground
This is a ground pin. It also acts as a reference for the logic pins, the OLED driving voltages, and the analogue circuits. It must be connected to external ground.</td></tr>
<tr><td>28
29
30</td><td>BPRE
GPRE
RPRE</td><td>I/O</td><td>External Voltage Reference for Pre-charge Signal
This is the precharge driving voltages for OEL driving segment pins respectively.
A zener diode should be connected between this pin and VSS.</td></tr>
<tr><td>31</td><td>V_{CC_C}</td><td>P</td><td>Power Supply for OEL Panel
This is the most positive voltage supply pin of the chip. It must be connected to external source.</td></tr>
<tr><td>32</td><td>V_{CC_R}</td><td>P</td><td>Voltage Output High Level for Scan Signal
This is the scan driver power supply pin. A tantalum capacitor should be connected between this pin and VSS.</td></tr>
<tr><td>33</td><td>VSSH</td><td>P</td><td>Ground of OEL Panel.
This is the ground pins for analog circuits. It must be connected to external ground.</td></tr>
<tr><td>34</td><td>N.C(GND)</td><td>-</td><td>Reserved Pin (Supporting Pin).
The supporting pin can reduce the influences from stresses on the function pins. These pins must be connected to external ground as the ESD protection circuit.</td></tr>
</table>

4 BLOCK DIAGRAM



MCU Interface Selection: PS, C80
Pins connected to MCU interface: RSTB, WRB, RDB, CSB, A0, and D0~D7
C1, C3, C5: 0.1µF
C2, C4, C8: 4.7µF
C6, C9: 4.7µF / 25V Tantalum Capacitor
C7: 2.2µF
R1: 39kΩ
R2: 27kΩ
D1: 2.7V, 0.5W Zener Diode

4.1 TIMING CHARACTERISTICS

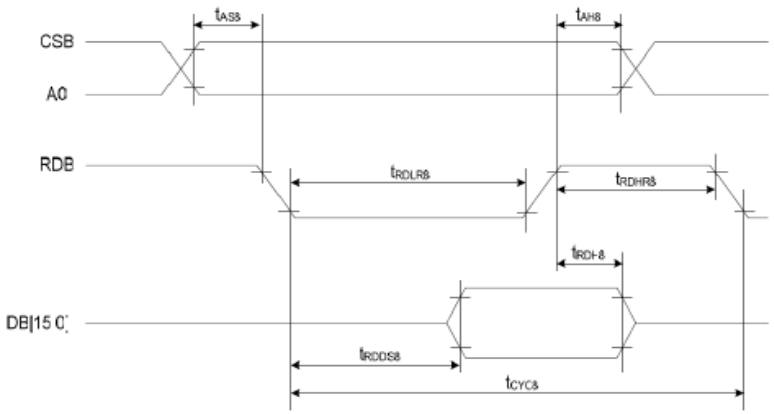
4.1.1 AC CHARACTERISTICS

4.1.1.1 80XX-Series MPU Parallel Interface Timing Characteristics:

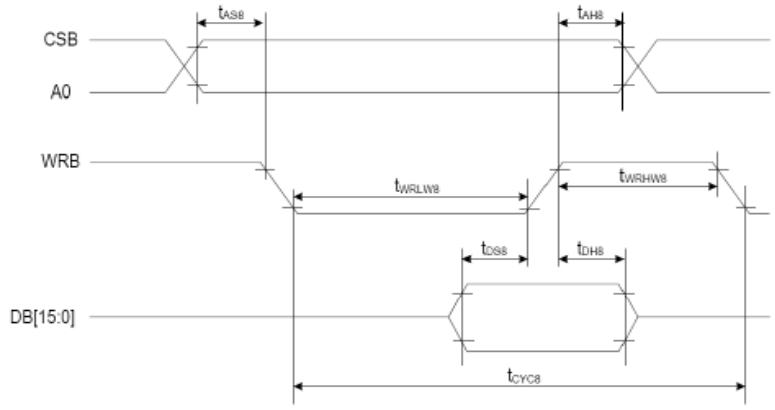
(V_{DD} = 2.8V , T_a = 25 ℃)

Symbol	Description	Min	Max	Unit	Port
t_{AS8}	Address Setup Timing	5	-	ns	CSB A0
t_{AH8}	Address Hold Timing	5	-	ns	
t_{CYC8}	System Cycle Timing	200	-	ns	RDB
t_{RDLR8}	Read "L" Pulse Width	90	-	ns	
t_{RDHR8}	Read "H" Pulse Width	90	-	ns	
t_{CYC8}	System Cycle Timing	100	-	ns	WRB
t_{WRLW8}	Write "L" Pulse Width	45	-	ns	
t_{WRHW8}	Write "H" Pulse Width	45	-	ns	
t_{RDD8}	Read Data Output Delay Time * CL = 15pF	-	60	ns	D[7:0]
t_{RDH8}	Data Hold Timing	0	60	ns	
t_{DS8}	Data Setup Timing	30	-	ns	
t_{DH8}	Data Hold Timing	10	-	ns	

* All the timing reference is 10% and 90% of V_{DDIO}.



(*Read Timing*)

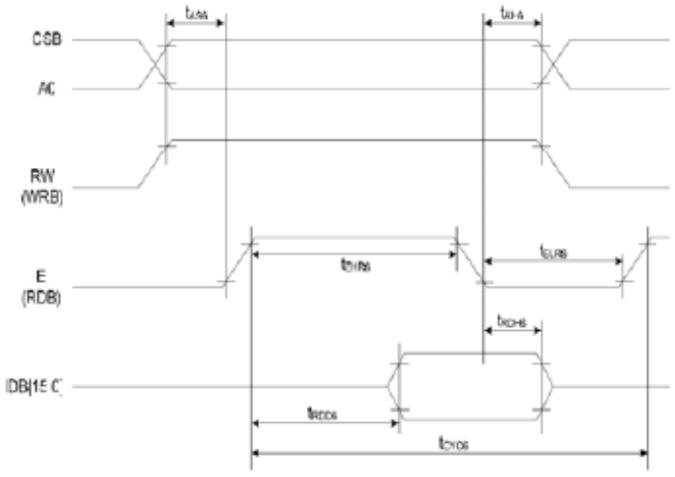


(*Write Timing*)

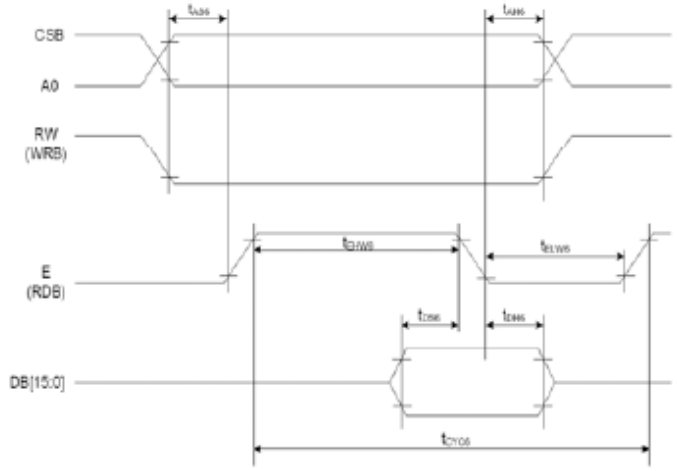
4.1.1.2 68XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description		Min	Max	Unit	Port
t_{AH6}	Address Setup Timing	(Read)	10	-	ns	CSB RS
		(Write)	5	-	ns	
t_{AS6}	Address Hold Timing	(Read)	10	-	ns	
		(Write)	5	-	ns	
t_{CYC6}	System Cycle Timing		200	-	ns	E
t_{ELR6}	Read "L" Pulse Width		90	-	ns	
t_{EHR6}	Read "H" Pulse Width		90	-	ns	
t_{CYC6}	System Cycle Timing		100	-	ns	
t_{ELW6}	Write "L" Pulse Width		45	-	ns	
t_{EHW6}	Write "H" Pulse Width		45	-	ns	
t_{RDD6}	Read Data Output Delay Time	* CL = 15pF	0	70	ns	D[7:0]
t_{RDH6}	Data Hold Timing		0	70	ns	
t_{DS6}	Data Setup Timing		40	-	ns	
t_{DH6}	Data Hold Timing		10	-	ns	

* All the timing reference is 10% and 90% of V_{DDIO}.



(*Read Timing*)

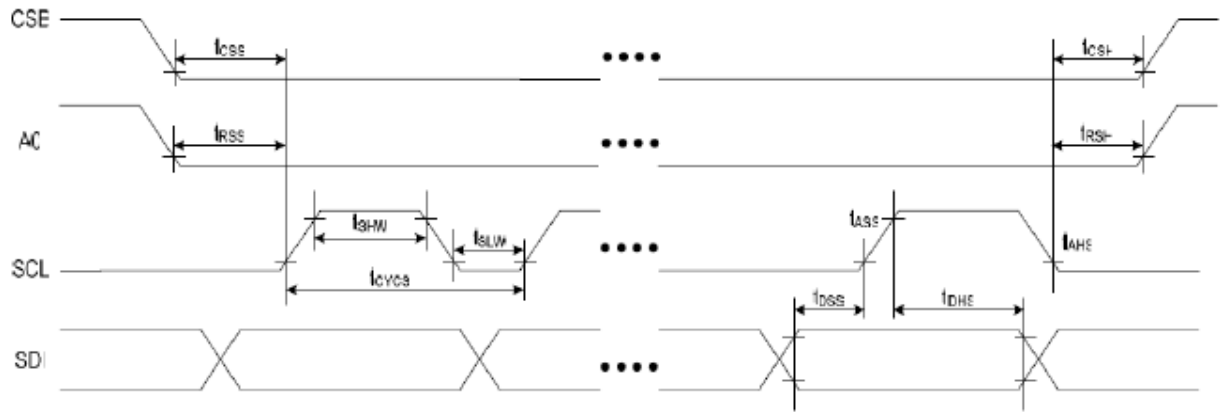


(*Write Timing*)

4.1.1.3 Serial Interface Timing Characteristics

Symbol	Description	Min	Max	Unit	Port
t_{CYCS}	Serial Clock Cycle	200	-	ns	SCL
t_{SLW}	SCL "L" Pulse Width	90	-	ns	
t_{SHW}	SCL "H" Pulse Width	90	-	ns	
t_{DSS}	Data Setup Timing	25	-	ns	SDI
t_{DHS}	Data Hold Timing	25	-	ns	
t_{CSS}	CSB-SCL Timing	25	-	ns	CSB
t_{CSH}	CSB-Hold Timing	25	-	ns	
t_{RSS}	RS-SCL Timing	25	-	ns	A0
t_{RSH}	RS-Hold Timing	25	-	ns	

* All the timing reference is 10% and 90% of V_{DDIO}.



5 OPTICAL SPECIFICATION

5.1 OPTICAL CHARACTERISTICS

Characteristics	Symbol	Condition	Min	Typ	Max	Unit
Brightness	L_{br}	Note 1	80	100	-	cd/m^2
C.I.E.(White)	(X)	C.I.E. 1931	0.26	0.30	0.34	-
	(Y)		0.29	0.33	0.37	
C.I.E.(Red)	(X)	C.I.E. 1931	0.60	0.64	0.68	-
	(Y)		0.30	0.34	0.38	
C.I.E.(Green)	(X)	C.I.E. 1931	0.27	0.31	0.35	-
	(Y)		0.58	0.62	0.66	
C.I.E.(Blue)	(X)	C.I.E. 1931	0.10	0.14	0.18	
	(Y)		0.12	0.16	0.20	
Dark Room Contrast	CR		-	>10,000:1	-	-
View Angle				Free	-	degree

Note 1: Optical measurement taken at V_{DD} = 2.8V, V_{CC} = 12.0V
Software configuration follows Section 5.4 Initialization.

6 FUNCTIONAL SPECIFICATION

6.1 COMMANDS

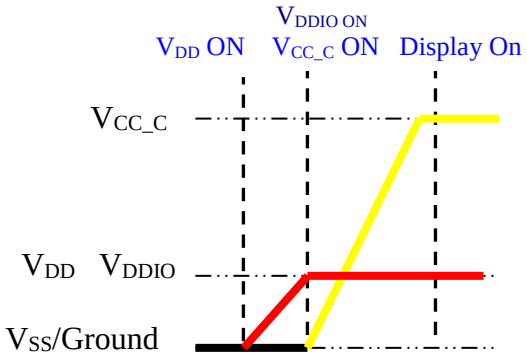
Please refer to the Technical Manual for the SEPS114A

6.2 POWER UP/DOWN SEQUENCE

To protect panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the panel enough time to complete the action of charge and discharge before/after the operation.

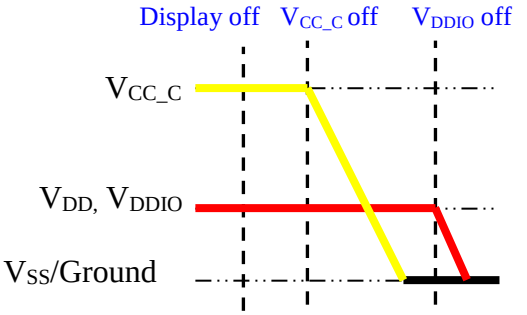
6.2.1 POWER UP SEQUENCE:

1. Power up V_{DD} & V_{DDIO}
2. Send Display off command
3. Initialisation
4. Clear Screen
5. Power up V_{CC_C}
6. Delay 100ms
   (When V_{CC_C} is stable)
7. Send Display on command



6.2.2 POWER DOWN SEQUENCE:

1. Send Display off command
2. Power down V_{CC_C}
3. Delay 100ms
   (When V_{CC_C} reaches 0 and panel is completely discharged)
4. Power down V_{DD} & V_{DDIO}



Note:
1) Since an ESD protection circuit is connected between V_{DD} and V_{CC_C} inside the driver IC, V_{CC_C} becomes lower than V_{DD} & V_{DDIO} whenever V_{DD} & V_{DDIO} is ON and V_{CC_C} is OFF.
2) VCC should be kept float (disabled) when it is OFF.
3) Power Pins (V_{DD}, V_{DDIO}, V_{CC_C}) can never be pulled to ground under any circumstance.
4) V_{DD} & V_{DDIO} should not be power down before V_{CC_C} is powered down.

6.3 RESET CIRCUIT

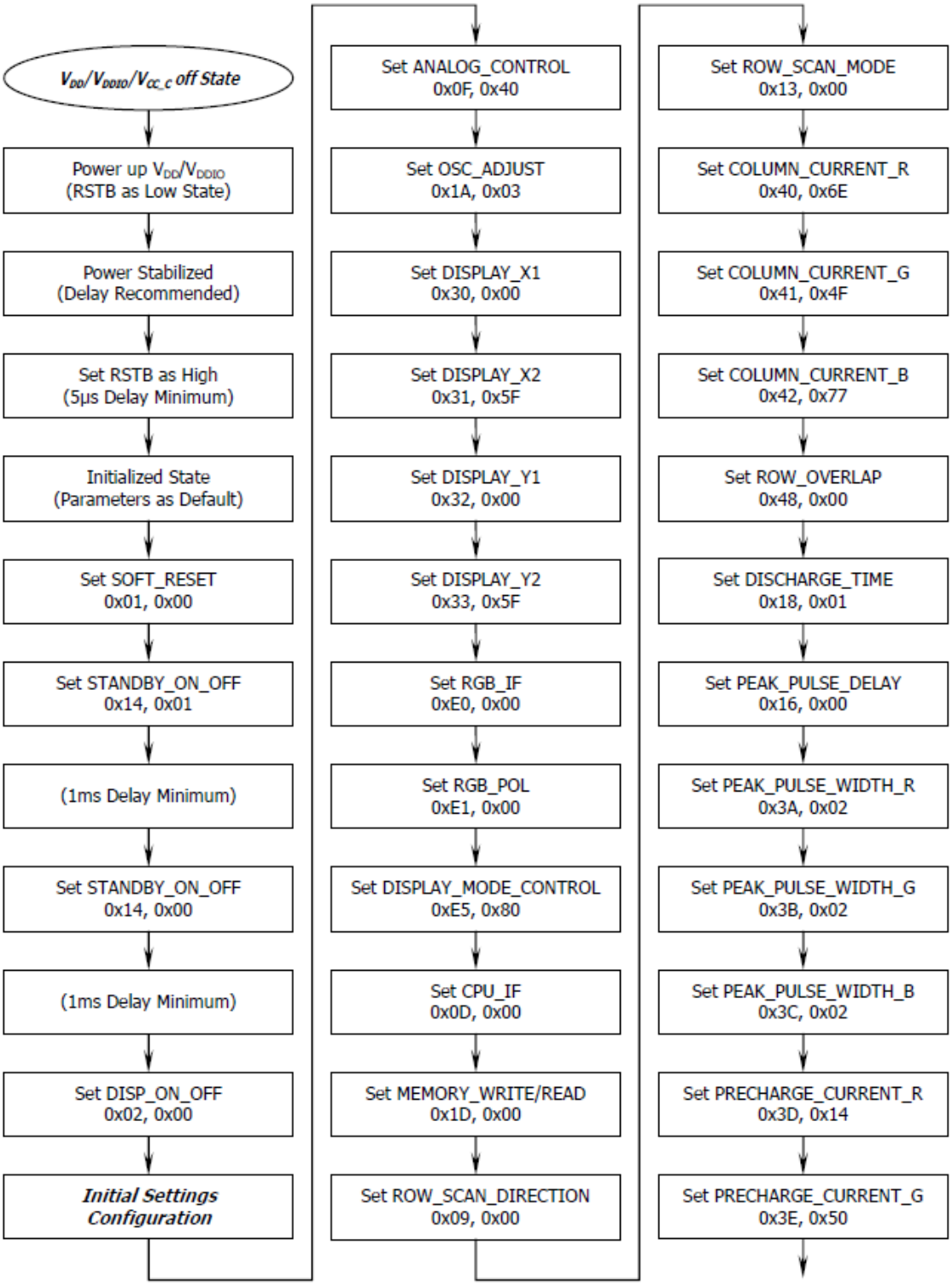
When RSTB input is low, the chip is initialized with the following status:

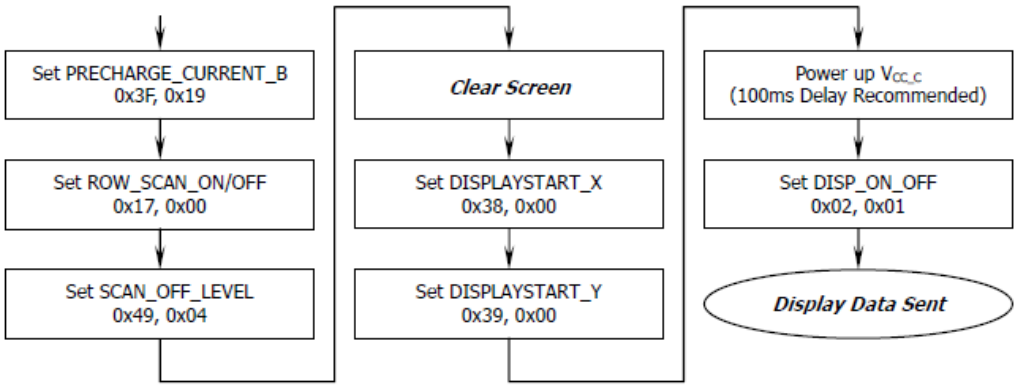
1. Standby Mode: On
2. Frame Frequency: 95Hz
3. Oscillation: Internal Oscillator Off
4. DDRAM Write Horizontal Address: XS = 0x00, XE = 0x5F
5. DDRAM Write Vertical Address: YS = 0x00, YE = 0x5F
6. Display Data RAM Write: MDIR1 = 0, MDIR0 = 0, VH = 0
7. Row Scan Shift Direction: R0, R1, … , R94, R95
8. Column Data Shift Direction: C0, C1, … , C286, C287
9. Display On/Off: Off
10. Panel Display Size: FX = 0x00, TX = 0x5F, FY = 0x00, TY = 0x5F
11. Display Data RAM Read Column/Row Address: DX = 0x00, DY = 0x00
12. Discharge Time: 8 Clock
13. Peak Pulse Delay: 5 Clock
14. Peak Pulse Width Time (R/G/B): 5 Clock
15. Precharge Current (R/G/B): 0uA
16. Driving Current (R/G/B): 0uA

6.4 ACTUAL APPLICATION EXAMPLE

Command usage and explanation of an actual example

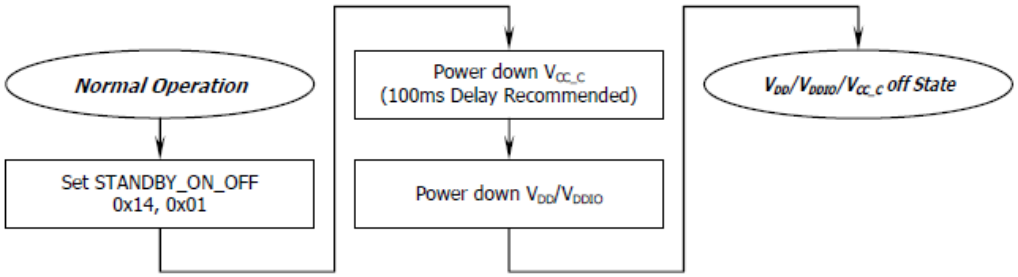
<Power up Sequence>



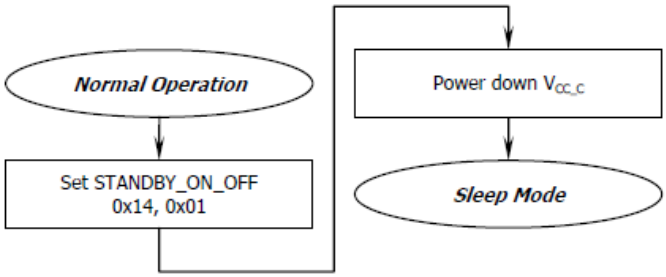


If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

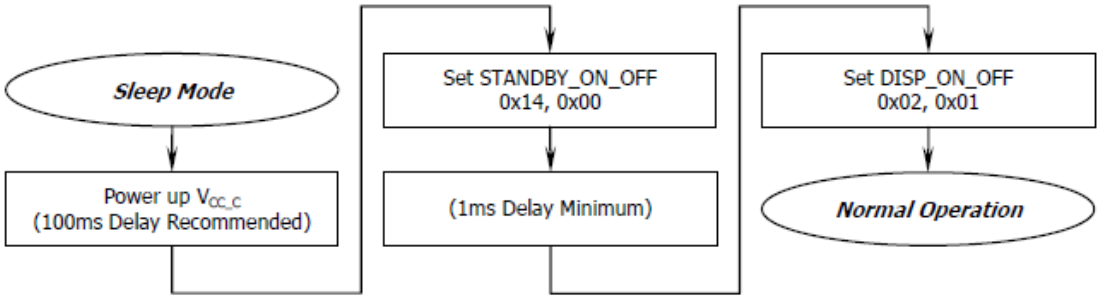
<Power down Sequence>

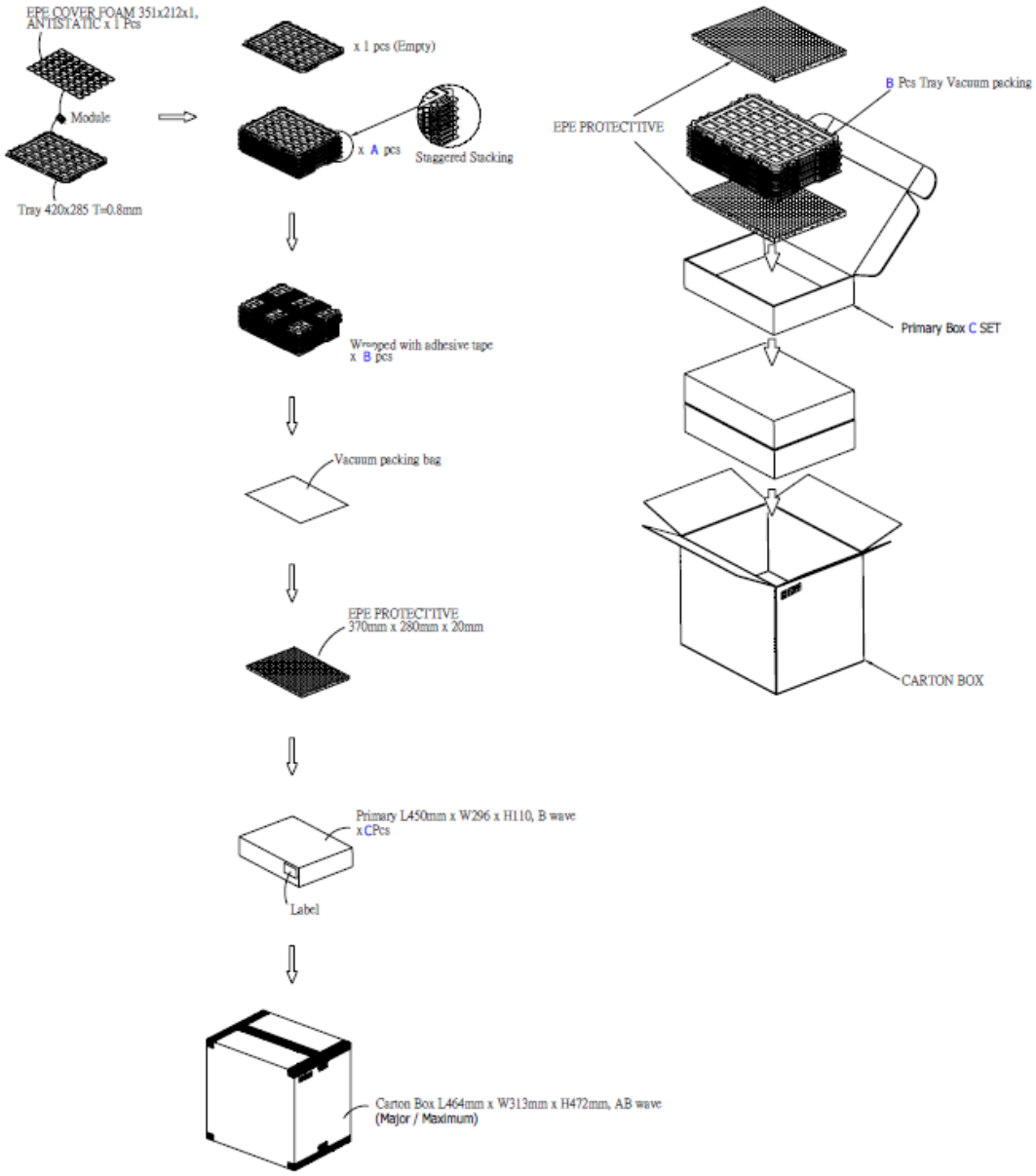


<Entering Sleep Mode>



<Exiting Sleep Mode>





Item		Quantity	
Module		**675**	**per Primary Box**
Holding Trays	**(A)**	**15**	**per Primary Box**
Total Trays	**(B)**	**16**	**per Primary Box (Including 1 Empty Tray)**
Primary Box	**(C)**	**1~4**	**per Carton (4 as Major / Maximum)**

6.5 LABELLING & MARKING

DENSITRON DD-9696FC-1A TW YY MM

7 QUALITY ASSURANCE SPECIFICATION

7.1 CONFORMITY

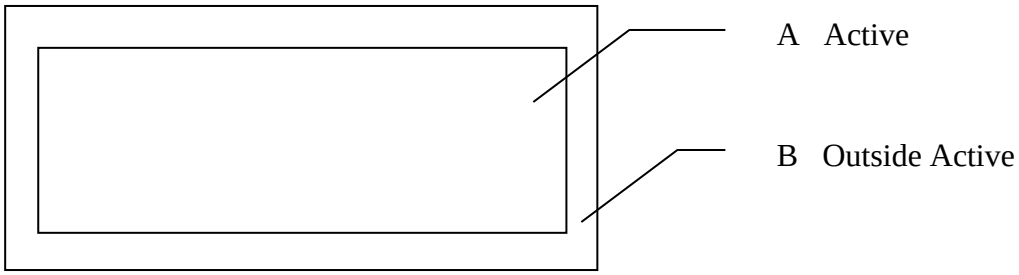
The performance, function and reliability of the shipped products conform to the Product Specification.

7.2 DELIVERY ASSURANCE

7.2.1 DELIVERY INSPECTION STANDARDS

IPC-AA610, class 2 electronic assemblies standard

7.2.2 Zone definition



7.2.3 Visual inspection

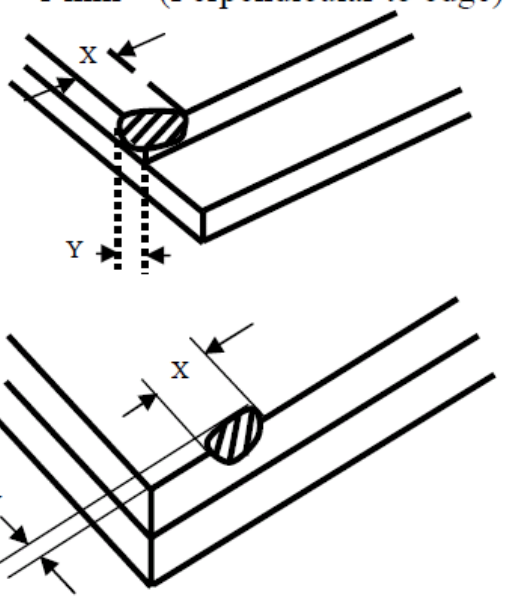
Test and measurement to be conducted under following conditions：

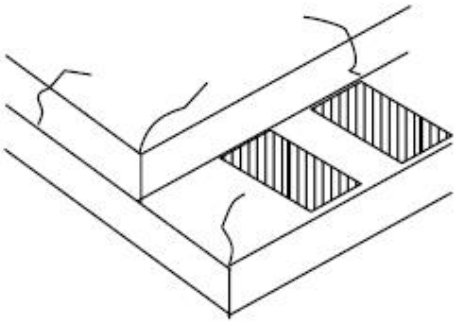
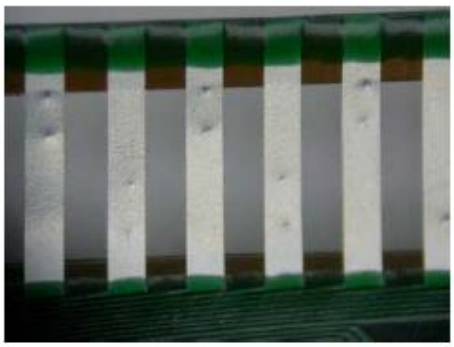
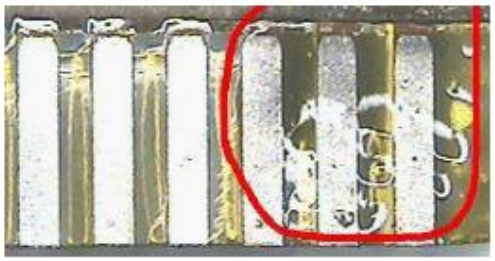
Temperature:	23±5℃
Humidity:	55±15%RH
Fluorescent lamp:	30 W
Distance between the Panel & Eyes of the Inspector:	≧30cm
Distance between the Panel & the lamp:	≧50cm

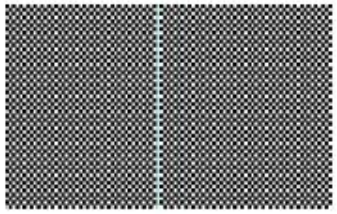
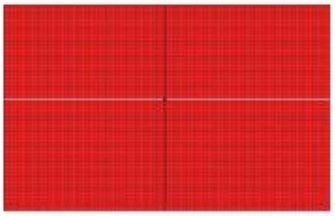
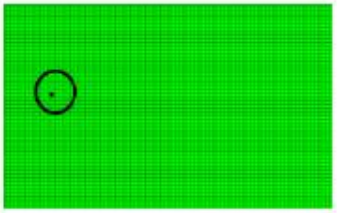
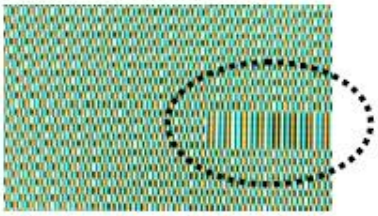
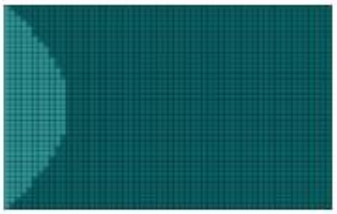
Finger glove (or finger cover) must be worn by the inspector.
Inspection table or jig must be anti-electrostatic

7.2.4 Standard of appearance inspection

Partition	AQL	Definition
Major	0.65	Defects in Pattern Check (Display On)
Minor	1.0	Defects in Cosmetic Check (Display Off)

Check Item	Classification	Criteria
Panel General Chipping	Minor	X > 6 mm (Along with Edge) Y > 1 mm (Perpendicular to edge) 

Check Item	Classification	Criteria
Panel Crack	Minor	Any crack is not allowable. 
Copper Exposed (Even Pin or Film)	Minor	Not Allowable by Naked Eye Inspection
Film or Trace Damage	Minor	
Terminal Lead Prober Mark	Acceptable	
Glue or Contamination on Pin (Couldn't Be Removed by Alcohol)	Minor	
Ink Marking on Back Side of panel (Exclude on Film)	Acceptable	Ignore for Any

Check Item	Classification	Criteria
Bright Line	Major	
Missed Line	Major	 
Pixel Short	Major	
Darker Pixel	Major	
Wrong Display	Major	
Un-Uniform (Luminance Variation within a Display)	Major	

7.3 DEALING WITH CUSTOMER COMPLAINTS

7.3.1 Non-conforming analysis

Purchaser should supply Densitron with detailed data of non-conforming sample.
After accepting it, Densitron should complete the analysis in two weeks from receiving the sample.
If the analysis cannot be completed on time, Densitron must inform the purchaser.

7.3.2 Handling of non-conforming displays

If any non-conforming displays are found during customer acceptance inspection which Densitron is clearly responsible for, return them to Densitron.
Both Densitron and customer should analyse the reason and discuss the handling of non-conforming displays when the reason is not clear.
Equally, both sides should discuss and come to agreement for issues pertaining to modification of Densitron quality assurance standard.

8 RELIABILITY SPECIFICATION

8.1 RELIABILITY TESTS

Test Item	Test Condition	Evaluation and assessment
High Temperature Operation	70℃, 240 hours	No abnormalities in function and appearance
Low Temperature Operation	-40℃, 240 hours	No abnormalities in function and appearance
High Temperature Storage	85℃, 240 hours	No abnormalities in function and appearance
Low Temperature Storage	-40℃, 240 hours	No abnormalities in function and appearance
High Temperature & High Humidity Storage(Operation)	60℃, 90%RH, 120 hours	No abnormalities in function and appearance
Thermal Shock	24 cycle of -40℃ 1 Hour, R.T. 5 min, 85℃ 1 Hour	No abnormalities in function and appearance

- The samples used for above tests do not include polarizer.
- No moisture condensation is observed during tests.

8.1.1 FAILURE CHECK STANDARD

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure teat at 23±5 ℃； 55±15% RH

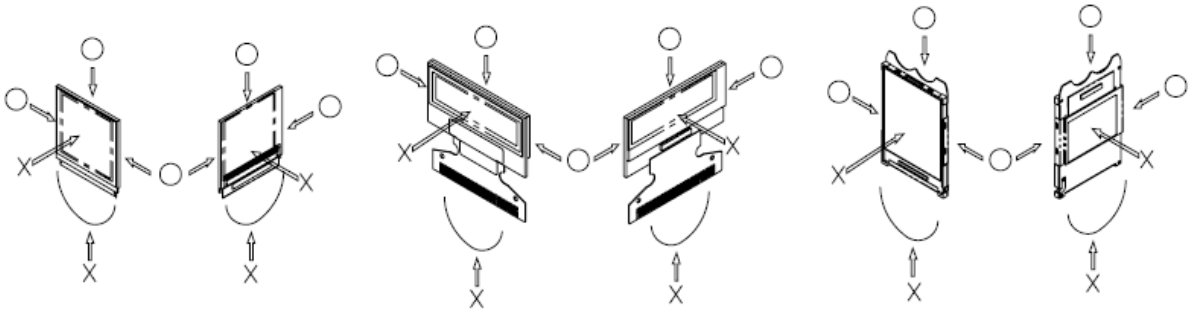
8.2 FAILURE CHECK STANDARD

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5 ℃; 55±15% RH.

9 HANDLING PRECAUTIONS

9.1 HANDLING PRECAUTIONS

1) Since the display panel is being made of glass, do not apply mechanical impacts such us dropping from a high position.
2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.
3) If pressure is applied to the display surface or its neighborhood of the OEL display module, the cell structure may be damaged and be careful not to apply pressure to these sections.
4) The polarizer covering the surface of the OEL display module is soft and easily scratched. Please be careful when handling the OEL display module.
5) When the surface of the polarizer of the OEL display module has soil, clean the surface. It takes advantage of by using following adhesion tape.
   * Scotch Mending Tape No. 810 or an equivalent
   Never try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy.
   Also, pay attention that the following liquid and solvent may spoil the polarizer:
   * Water
   * Ketone
   * Aromatic Solvents
6) Hold OEL display module very carefully when placing OEL display module into the system housing. Do not apply excessive stress or pressure to OEL display module. And, do not over bend the film with electrode pattern layouts. These stresses will influence the display performance. Also, secure sufficient rigidity for the outer cases.



7) Do not apply stress to the LSI chips and the surrounding molded sections.
8) Do not disassemble nor modify the OEL display module.
9) Do not apply input signals while the logic power is off.
10) Pay sufficient attention to the working environments when handing OEL display modules to prevent occurrence of element breakage accidents by static electricity.
    * Be sure to make human body grounding when handling OEL display modules.
    * Be sure to ground tools to use or assembly such as soldering irons.
    * To suppress generation of static electricity, avoid carrying out assembly work under dry environments.

* Protective film is being applied to the surface of the display panel of the OEL display module. Be careful since static electricity may be generated when exfoliating the protective film.

11) Protection film is being applied to the surface of the display panel and removes the protection film before assembling it. At this time, if the OEL display module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).
12) If electric current is applied when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

9.2 STORAGE PRECAUTIONS

1) When storing OEL display modules, put them in static electricity preventive bags avoiding exposure to direct sun light nor to lights of fluorescent lamps, etc. and, also, avoiding high temperature and high humidity environments or low temperature (less than 0°C) environments. (We recommend you to store these modules in the packaged state when they were shipped from Densitron Technologies Plc.) At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.
2) If electric current is applied when water drops are adhering to the surface of the OEL display module, when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

9.3 DESIGNING PRECAUTIONS

1) The absolute maximum ratings are the ratings which cannot be exceeded for OEL display module, and if these values are exceeded, panel damage may be happen.
2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the VIL and VIH specifications and, at the same time, to make the signal line cable as short as possible.
3) We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (VDD). (Recommend value: 0.5A)
4) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighboring devices.
5) As for EMI, take necessary measures on the equipment side basically.
6) When fastening the OEL display module, fasten the external plastic housing section.
7) If power supply to the OEL display module is forcibly shut down by such errors as taking out the main battery while the OEL display panel is in operation, we cannot guarantee the quality of this OEL display module.
8) The electric potential to be connected to the rear face of the IC chip should be as follows: US2066
   * Connection (contact) to any other potential than the above may lead to rupture of the IC.

9.4 OTHER PRECAUTIONS

1) When an OEL display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur. Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored. Also, there will be no problem in the reliability of the module.
2) To protect OEL display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the OEL display modules.
   * Pins and electrodes
   * Pattern layouts such as the FPC
3) With this OEL display module, the OEL driver is being exposed. Generally speaking, semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if this OEL driver is exposed to light, malfunctioning may occur.
   * Design the product and installation method so that the OEL driver may be shielded from light in actual usage.
   * Design the product and installation method so that the OEL driver may be shielded from light during the inspection processes.
4) Although this OEL display module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed. It therefore is necessary to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.
5) We recommend you to construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.

9.5 PRECAUTIONS WHEN DISPOSING OF THE OEL DISPLAY MODULES

1) Request the qualified companies to handle industrial wastes when disposing of the OEL display modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.

10 SUPPORTED ACCESSORIES

10.1 DUO KIT

Densitron has developed an easy to use yet powerful development and demonstration tool for driving its range of Passive matrix OLED displays from the USB port of a PC.
DUO (Densitron USB OLED) kit is hot pluggable and does not require extra cables or power supply to run, allowing users to be up and running in minutes.

The kit consists of an OLED display with transition Board, USB controller card, mini USB cable and a CD with software application and drivers.

Part number: UNDER DEVELOPMENT

10.2 TRANSITION BOARD CARD

A Transition board card is like a daughterboard which is meant to be a circuit board for connections between the baseboards (V-DUO and DUO).
It has connector pins for interfacing between the display and the baseboards.
It also includes the OLED display.
Part number: UNDER DEVELOPMENT

10.3 CONNECTOR BOARD CARD

A Connector board is a daughterboard which allows a connection between customer's microprocessor or microcontroller (customer's system) to the display.
Part number: EVK-CONNECT-033

10.4 CONNECTOR

Type: hot bar soldering process
No. of connections: 34
Pitch: 0.70mm