LIQUID CRYSTAL DISPLAY MODULE

Product Specification

CUSTOMER	**Standard**
CUSTOMER PART NUMBER	
PRODUCT NUMBER	**DBC-32024035-1A0**

Product Mgr	Design Eng
Bruno Recaldini	**Luo Luo**
Date: 15-Feb-12	Date: 15-Feb-12

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REVISION RECORD

Rev.	Date	Page	Chapt.	Comment	ECN no.
1	19.02.2010			First Issue	
1.1	15-Feb-12	7	2.3	Added Serial Label / Print	

1 MAIN FEATURES

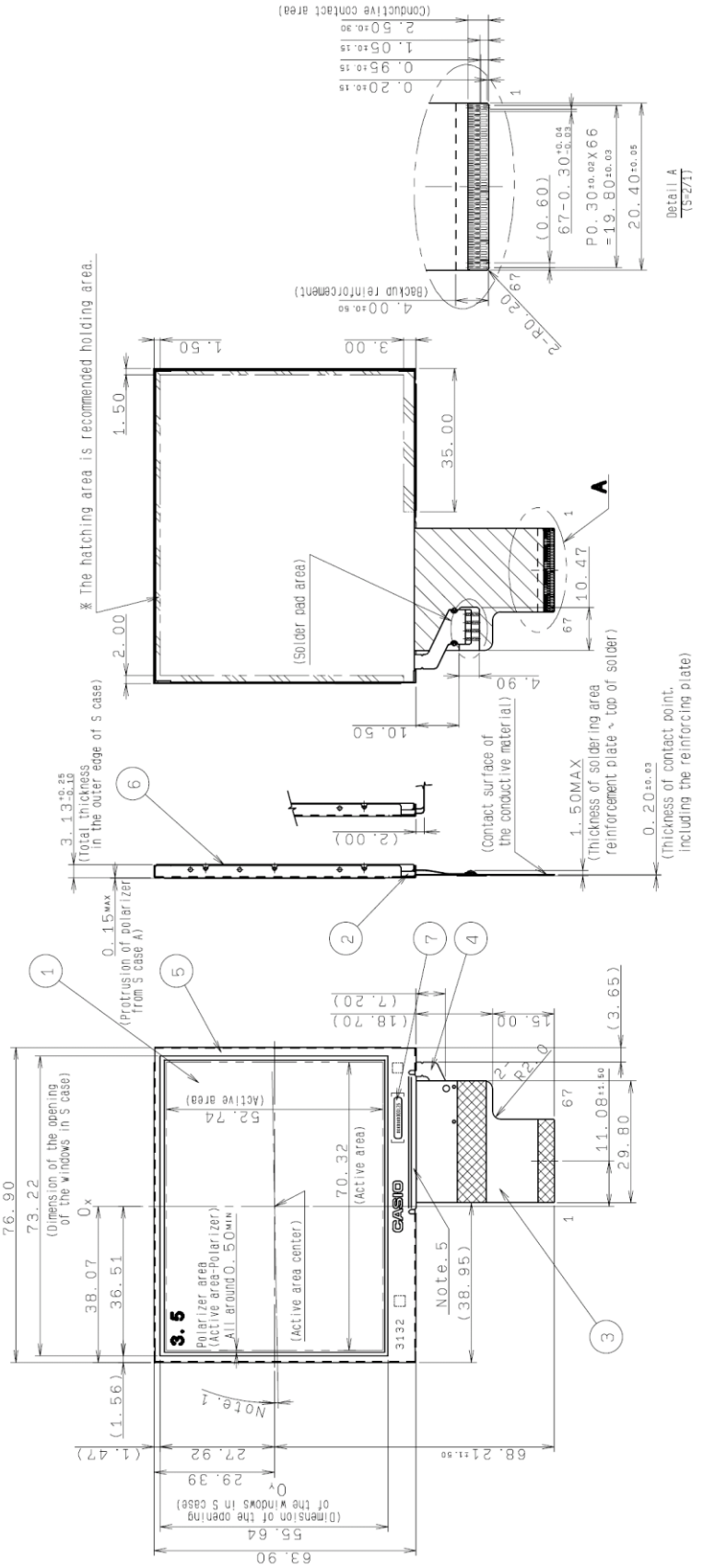
ITEM	CONTENTS
Screen Size	3.5” Diagonal
Display Format	320 x RGB x 240 Dots
N° of Colour	16.7 million
Overall Dimensions	76.90 mm (H) x 63.90 mm (V) x 3.13 mm (D)
Active Area	70.32 mm (H) x 52.74 mm (V)
LCD Type	TFT
Mode	Sunlight Readable
Interface	6-bit / 8-bit RGB, parallel input
Backlight Type	LED
Operating Temperature	-20°C ~ +70°C
Storage Temperature	-30°C ~ +80°C
RoHS compliant	Yes

2 MECHANICAL SPECIFICATION

2.1 MECHANICAL CHARACTERISTICS

ITEM	CHARACTERISTIC	UNIT
Display Format	320 x RGB x 240 Dots	Dots
Overall Dimensions	76.90 mm (H) x 63.90 mm (V) x 3.13 mm (D)	mm
Bezel Opening Area	73.22 (H) x 55.64 (V)	mm
Active Area	70.32 mm (H) x 52.74 mm (V)	mm
Dot Pitch	73.25 (H) x RGB x 219.75 (V)	µm
Weight	33.0	g

2.2 MECHANICAL DRAWING



Note 1. Angular deviation of LCD cell from the TFT-LCD monitor's reference axis shall be less than ±40°.
Note 2. S label is affixed in the area shown in the drawing. The thickness of S label will be added to that of S case's surface.
Note 3. Recommended FPC connectors. Kyocera Elco part number 04 6281 267 2X2 846+ (lower contact); HIROSE, part number: FH26G-67S-0.3SHBW(05) (lower contact)
Note 4. Protective film is affixed on front surface of the screen. Location tolerance of the protective film shall be ±1.5 mm to the polariser.
Note 5. Exercise care not to apply any forces to the cable holder of the S case A
Note 6. Refer to "QUALITY ASSURANCE SPECIFICATION" about the appearance specification of a polarizer.

1. LCD
2. S-Case B
3. LCD-FPC
4. LED-FPC
5. S-Case A
6. S-Case C
7. S Label

2.3 SERIAL LABEL / PRINT

The label / print indicates the least significant digit of manufacture year (1digit), manufacture month with below alphabet (1letter), model code (4 or 5 characters), serial number (6 digits).

* Label / Print Contents

*	*	****(*)	******
a	b	c	d

where:

a The least significant digit of manufacturing year

b Manufacturing Month:
Jan-A, Feb-B, Mar-C, Apr-D, May-E, Jun-F, Jul-G, Aug-H, Sep-I, Oct-J, Nov-K, Dec-L

c Model code
35DZC →Made in Japan
35EBC →Made in Malaysia
35EAC →Made in China

d Serial number, like “000125”

Examples:

Made in Japan
2D35DZC000125
means "manufactured in April 2012, model 35DZC, serial number 000125"

Made in Malaysia
2D35EBC000125
means "manufactured in April 2012, model 35EBC, serial number 000125"

Made in China
2D35EAC000125
means "manufactured in April 2012, model 35EAC, serial number 000125"

3 ELECTRICAL SPECIFICATION

3.1 ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Condition	Min	Max	Unit	Applicable terminal
Supply Voltage	VDD	Ta= 25°C	-0.3	6.0	V	VDD
Input Voltage 1 for Logic	VI1		-0.3	VDD+0.3	V	POCB,CLK,VSYNC, HSYNC,D[27:20], D[17:10], D[07:00], MODE
Input Voltage 2 for Logic	VI2		-0.3	6.0	V	CS/STBY,DI/DE, SCK/REV

3.2 ELECTRICAL CHARACTERISTICS

Item	Symbol	Condition	Min	Typ	Max	Unit	Applicable terminal
Supply Voltage	VDD	VDD	2.7	3.0	3.6	V	VDD
Input Voltage 1 for Logic	VI1	VDD= 2.7~3.6V	0	--	VDD	V	POCB,CLK, VSYNC, HSYNC, D[27:20], D[17:10], D[07:00], MODE
Input Voltage21 for Logic	VI2		0	--	VDD	V	CS/STBY,DI/DE , SCK/REV
Common electrode centre voltage [Note 1]	VCOMDC	MODE="VSS" VDCOMDC[5:0] =16h-C3h	1.48	1.86	2.24	V	COMDC
		MODE="VDD"	1.48	1.86	2.24	V	

Note1: Common-electrode centre voltage indicates that optimum VCOMDC value lies within the bound of these voltages, but it does not mean the whole range of voltages are the optimum VCOMDC value

(Unless otherwise noted, Ta=25°C, VDD=3.0V, VSS=0V)

Item	Symbol	Condition	Min	Typ	Max	Unit	Applicable terminal
Schmitt Threshold voltage	VP	VDD= 2.7~3.6V	0.47xVDD	0.60xVDD	0.73xVDD	V	CS/STBY,DI/DE, SCK/REV, VSYNC, HSYNC, D[27:20], D[17:10], D[07:00], CLK, POCB
	VN		0.30xVDD	0.43xVDD	0.56xVDD	V	
	VH		0.08xVDD	0.17xVDD	0.27xVDD	V	
Input signal voltage	VIH		0.7xVDD	-	VDD	V	MODE
	VIK		0	-	0.3xVDD	V	
Pull Up Resister Value	Rpu		45	91	182	kΩ	POCB
Pull Down Resister Value	Rpd		45	91	182	kΩ	MODE
Output voltage 1	VDD2		4.8	5.6	6.1	V	VDD2
Output voltage 2	VGH		12.5	13.3	13.5	V	VGH
Output voltage 3	VGL		-13.5	-13.3	-12.5	V	VGL
Output voltage 4	VOH	Io = -1.0mA	VDD-0.5	-	VDD	V	BLON
	VOL	Io = 1.0mA	0	-	0.5	V	
Operating Current	IDD	fCLK= 6.75MHz Colour bar display BRIGHT[5:0] CONTRAST [3:0] = Initial value	-	8.0	15.0	mA	VDD
Standby Current	IDDs	MODE- “VSS”, Other input with constant voltage	-	11.0	30.0	μA	
		MODE- “VDD”, Other input with constant voltage	-	44.0	96.0		

At “MODE” = “VSS”

(Unless otherwise noted, Ta=25°C, VDD=3.0V, VSS=0V)

Item	Symbol	Condition	Min	Typ	Max	Unit	Applicable terminal
VcomDC Adjusted value	VCOMDC	VCOMDC[5:0]=00h	0.94	1.04	1.14	V	COMDC
		VCOMDC[5:0]=1Fh	1.56	1.66	1.76	V	
		VCOMDC[5:0]=3Ch	2.14	2.24	2.34	V	

(Unless otherwise noted, Ta=25°C, VDD=3.0V, VSS=0V)

Item	Symbol	Condition		Min	Typ	Max	Unit
BRIGHT Adjusted value	VLCD	BRIGHT[5:0]=00h	D[*7:0]=00h	4.10	4.25	4.40	V
		CONTRAST[3:0]=Eh	D[*7:0]=FFh	0.92	1.07	1.22	
		BRIGHT[5:0]=1Ah	D[*7:0]=00h	3.58	3.73	3.88	
		CONTRAST[3:0]=Eh	D[*7:0]=FFh	0.40	0.55	0.70	
		BRIGHT[5:0]=2Eh	D[*7:0]=00h	3.18	3.33	3.48	
		CONTRAST[3:0]=Eh	D[*7:0]=FFh	0.00	0.15	0.30	
CONTRAST Adjusted value	VLCD	CONTRAST [3:0]=0h VLCD(D[*7:0]=00h)-VLDC(D[*7:0]=FFh)		1.35	1.50	1.65	V
		CONTRAST [3:0]=Eh VLCD(D[*7:0]=00h)-VLDC(D[*7:0]=FFh)		3.03	3.18	3.33	
		CONTRAST [3:0]=Fh VLCD(D[*7:0]=00h)-VLDC(D[*7:0]=FFh)		3.15	3.30	3.45	

3.3 INTERFACE PIN ASSIGNMENT

3.3.1 LCM PIN Assignment

Pin No.	Symbol	Function	
		Mode (No. 34 pin) = “VSS”	Mode (No. 34 pin) = “VDD”
1	VCOM	Common-electrode driving signal	
2	D27	Display data (B) 00h: Black D20:LSB D27:MSB Driver has internal gamma conversion.	Display data (B) 00h: Black D22:LSB D27:MSB Driver has internal gamma conversion.
3	D26		
4	D25		
5	D24		
6	D23		
7	D22		
8	D21		Short to VSS
9	D20		Short to VSS
10	D17	Display data (G) 00h: Black D10:LSB D17:MSB Driver has internal gamma conversion.	Display data (G) 00h: Black D12:LSB D17:MSB Driver has internal gamma conversion.
11	D16		
12	D15		
13	D14		
14	D13		
15	D12		
16	D11		Short to VSS
17	D10		Short to VSS
18	D07	Display data (R) 00h: Black D00:LSB D07:MSB Driver has internal gamma conversion.	Display data (R) 00h: Black D02:LSB D07:MSB Driver has internal gamma conversion.
19	D06		
20	D05		
21	D04		
22	D03		
23	D02		
24	D01		Short to VSS
25	D00		Short to VSS
26	BLON	Logic signal output for external backlight circuitry	OPEN
27	CS/STBY	CS: Chip select input for serial communication	STBY: Standby signal (Lo: Normal operation, Hi: Standby)
28	DI/DE	DI: Data input for serial communication	DE: Input data effective signal
29	SCK/REV	SCK: Clock input for serial communication	REV: Right/Left & Up/Down display reverse (Lo: normal display, Hi: reverse display)
30	VSYNC	Vertical sync signal input	Vertical sync signal input (negative polarity)
31	HSYNC	Horizontal sync signal input	Horizontal sync signal input (negative polarity)
32	CLK	Clock input signal	Clock input signal
33	VSS	GND	
34	MODE	Input specification selection input	

35	POCB	Power On clear (Lo: active)
36	NC	OPEN
37	RVDD	Internal power supply
38	COMDC	Common-electrode drive DC output
39	NC	OPEN
40	VSREF	Built-in DAC reference supply
41	C1P	Contacting terminal of capacitor for charge pump
42	C1M	Contacting terminal of capacitor for charge pump
43	C2M	Contacting terminal of capacitor for charge pump
44	C2P	Contacting terminal of capacitor for charge pump
45	VDD	Power supply input
46	COMOUT	Square wave output for common-electrode
47	VDD2	Internal power supply
48	VSS	GND
49	VSS	GND
50	VSS	GND
51	C3M	Contacting terminal of capacitor for charge pump
52	C3P	Contacting terminal of capacitor for charge pump
53	C4M	Contacting terminal of capacitor for charge pump
54	C4P	Contacting terminal of capacitor for charge pump
55	VVCOM	Voltage output for COMOUT
56	NC	OPEN
57	NC	OPEN
58	VGH	Positive supply for gate driver
59	C5P	Contacting terminal of capacitor for charge pump
60	C5M	Contacting terminal of capacitor for charge pump
61	VGL	Negative supply for gate driver
62	BLL2	LED drive power source 2 (Cathode side)
63	BLH2	LED drive power source 2 (Anode side
64	NC	OPEN
65	NC	OPEN
66	BLH1	LED drive power source 1 (Anode side)
67	BLL1	LED drive power source 1 (Cathode side

Recommended connector: Kyocera Elco 6281 series [04 6281 267 2x2 846+]
Hirose Electric FH26 series [FH26G-67S-0.3SHBW(05)]
As FCB cable has gold plated terminals, gilt finish contact shoe connector is recommended.

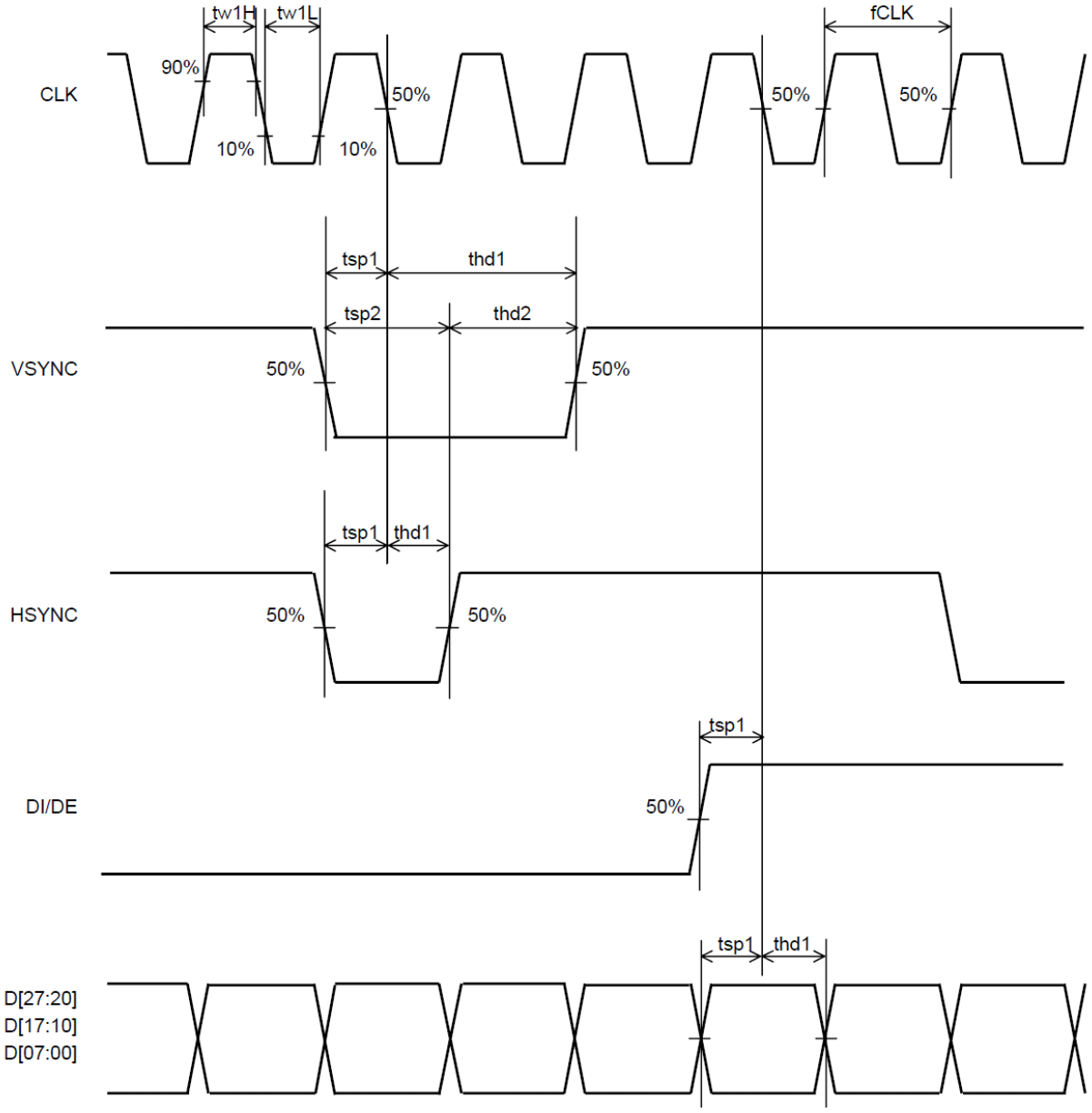
3.4 TIMING CHARACTERISTICS

3.4.1 AC Timing Characteristics

(Unless otherwise noted, Ta = 25°C, VDD = 3.0V, VSS = 0V)

Item	Symbol	Condition	Rating			Unit	Applicable terminal
			MIN	TYP	MAX		
CLK Low period	tw1L	0.1xVDD or less	20	-	-	ns	CLK
CLK High period	tw1H	0.9xVDD or more	20	-	-	ns	
Setup time 1	tsp1		10	-	-	ns	CLK, VSYNC, HSYNC, D[27:20], D[17:10], D[07:00], DI/DE [Note1]
Hold time 1	thd1		10	-	-	ns	
Setup time 2	tsp2		2	-	-	CLK	VSYNC, HSYNC
Hold time 2	thd2		2	-	-	CLK	
CLK frequency	fCLK		-	6.75	9.0	MHz	CLK

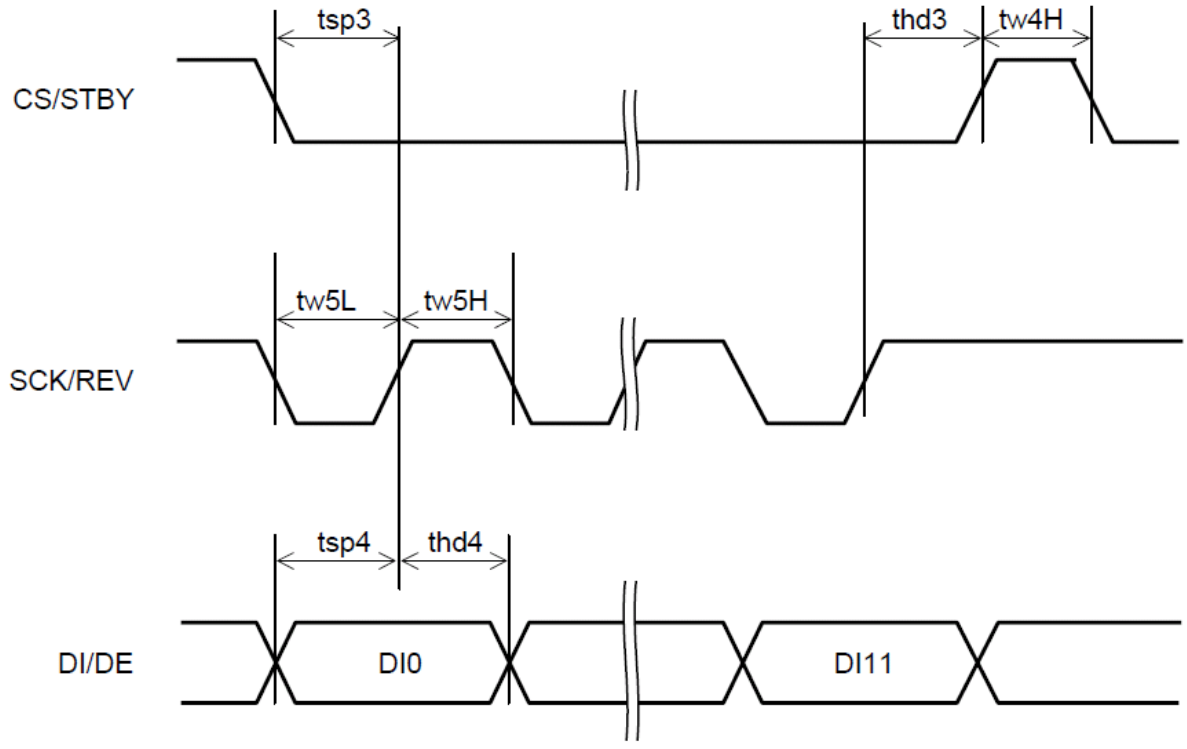
3.4.2 AC Timing Diagrams



3.4.3 Serial Communication Block (at “MODE” = “VSS”)

(Unless otherwise noted, Ta = 25°C, VDD = 3.0V, VSS = 0V)

Item	Symbol	Condition	Rating			Unit	Applicable terminal
			MIN	TYP	MAX		
CS setup time	tsp3		20	-	-	ns	CS/STBY
CS hold time	thd3		20	-	-	ns	
DI setup time	tsp4		20	-	-	ns	DI/DE
DI hold time	thd4		20	-	-	ns	
CS pulse high period	tw4H		20	-	-	ns	CS/STBY
SCK pulse low period	tw5L		20	-	-	ns	SCK/REV
SCK pulse high period	tw5H		20	-	-	ns	SCK/REV



Note: unless otherwise noted, each item is defined between each 50% point of signal amplitude.

3.4.4 Input Timing Characteristics

MODE = "VSS"

Item	Symbol	Rating			Unit	Applicable terminal
		MIN	TYP	MAX		
CLK frequency	fCLK	-	6.75	9.0	MHz	CLK
VSYNC frequency Note1	fVSYNC	54	60	66	Hz	VSYNC
Number of Frame Line	tv	-	262	291	H	VSYNC,HSYNC
VSYNC pulse width	tw2H	4CLK	3H	-		VSYNC,CLK
Vertical back porch	tvb	0 Note2	6	31	H	VSYNC, HSYNC, D[27:20], D[17:10], D[07:00]
Vertical display period	tvdp	-	240	-	H	
HSYNC frequency	fHSYNC	-	15.7	-	KHz	HSYNC
HSYNC signal cycle time	th	-	429	573	CLK	HSYNC, CLK
HSYNC pulse width	tw3H	2CLK	-	20µs		
Horizontal back porch	thb	5	42	-	CLK	HSYNC,CLK, D[27:20], D[17:10], D[07:00]
Horizontal display period	thdp	-	320	-	CLK	D[27:20], D[17:10], D[07:00], CLK

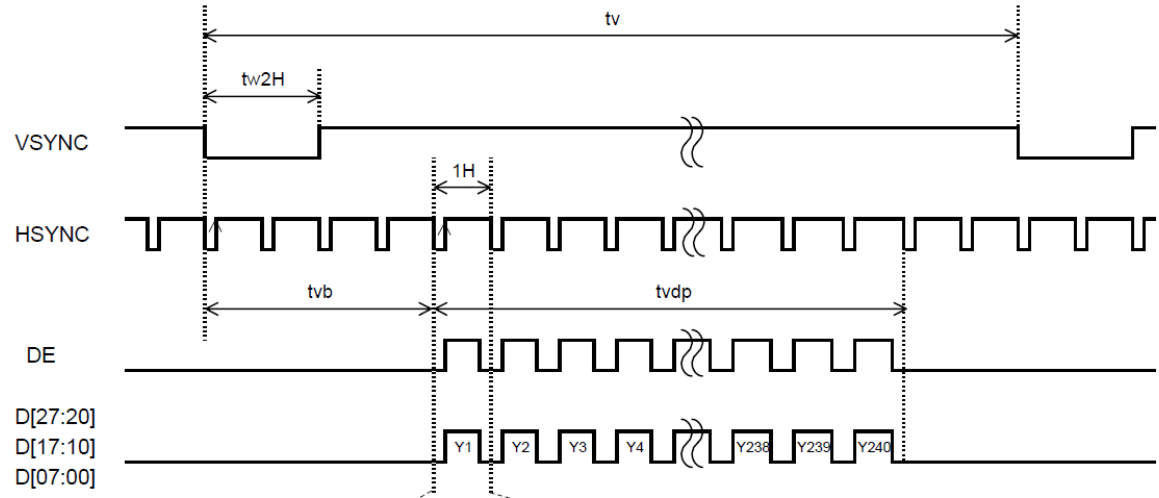
MODE = "VDD"

Item	Symbol	Rating			Unit	Applicable terminal
		MIN	TYP	MAX		
CLK frequency	fCLK	-	6.75	9.0	MHz	CLK
VSYNC frequency Note1	fVSYNC	54	60	66	Hz	VSYNC
Number of Frame Line	tv	-	262	291	H	VSYNC,HSYNC
VSYNC pulse width	tw2H	4CLK	3H	-		VSYNC,CLK
Vertical back porch	tvb	0 Note2	6	21 Note3	H	VSYNC, HSYNC, DE, D[27:22], D[17:12], D[07:02]
Vertical display period	tvdp	-	240	-	H	
HSYNC frequency	fHSYNC	-	15.7	-	KHz	HSYNC
HSYNC signal cycle time	th	-	429	573	CLK	HSYNC, CLK
HSYNC pulse width	tw3H	2CLK	-	20µs		
Horizontal back porch	thb	5	42	77 Note3	CLK	HSYNC,CLK, DE, D[27:22], D[17:12], D[07:02]
DE Pulse Width	tw4H	-	320	-	CLK	DE, CLK
Horizontal display period	thdp	-	320	-	CLK	D[27:22], D[17:12], D[07:02], CLK

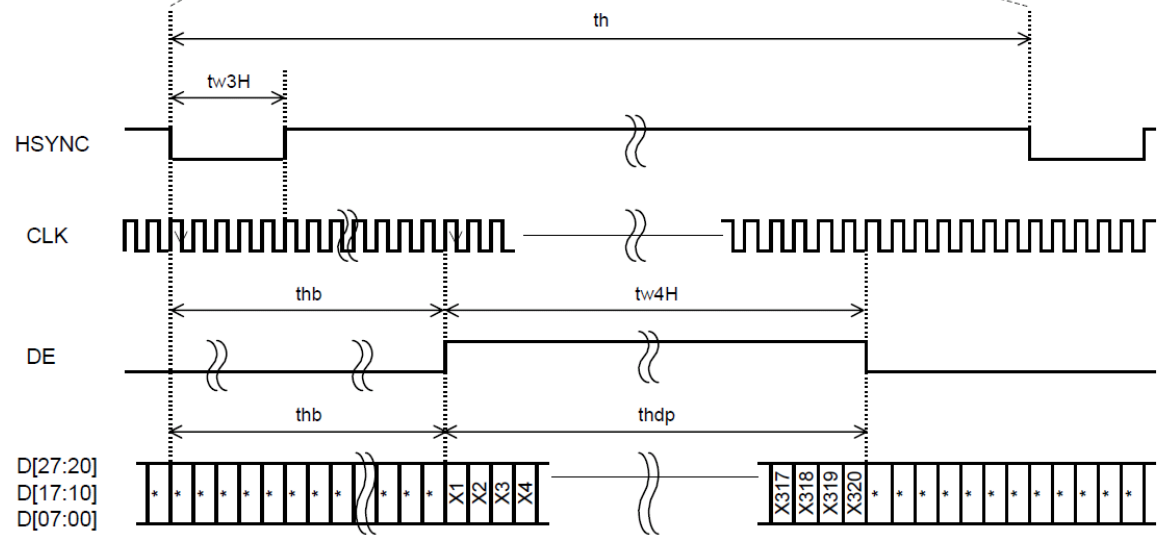
Note 1: This is recommended spec to get high quality picture on display.
Note 2: When Vertical Back Porch is "0" please use odd number for the setting of the total number of lines that compose one field.
Note 3: when DE keeps "Lo" for 21H and 77CLK or longer, start capturing data automatically from "22H and 78 CLK".

3.4.5 Driving Timing Chart

-Vertical Timing



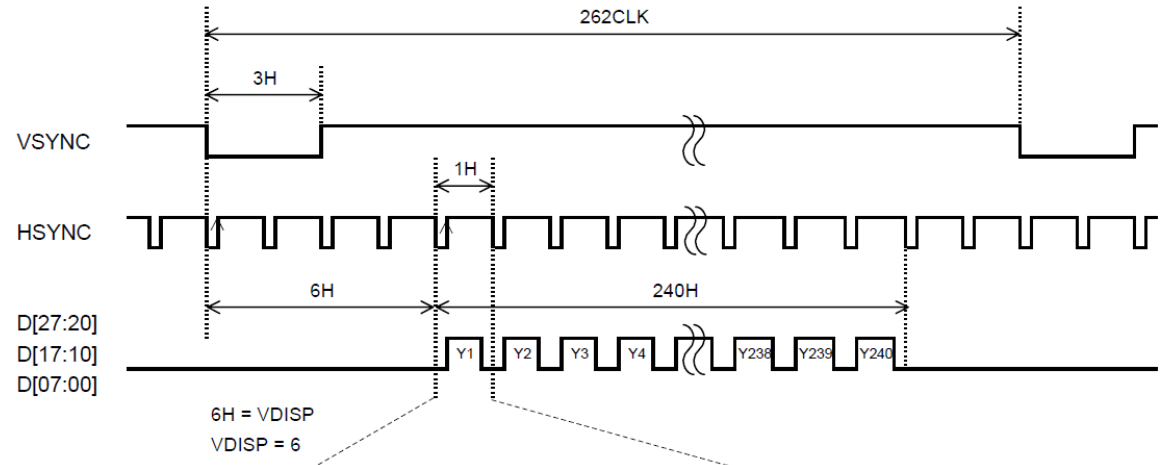
-Horizontal Timing



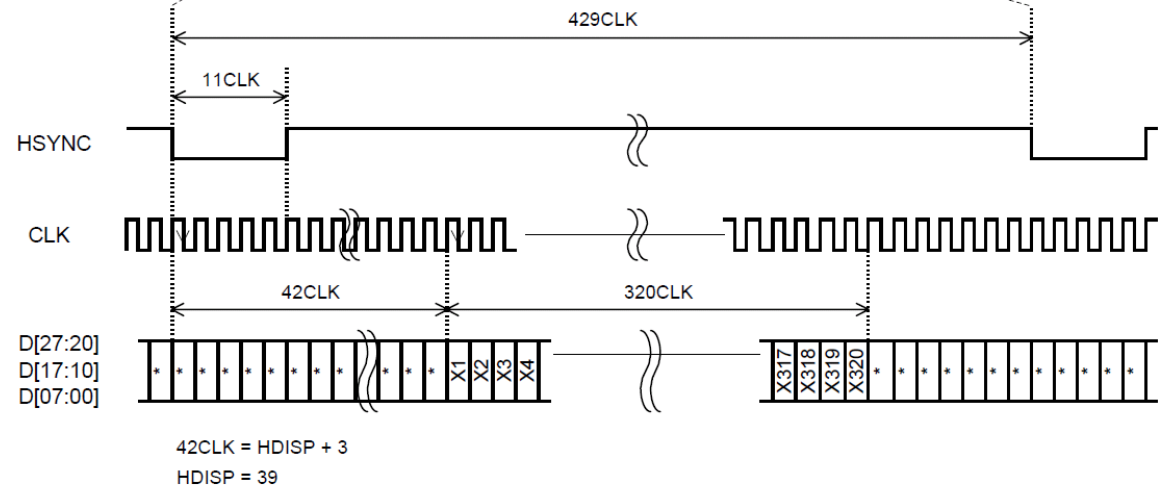
3.4.6 Example of Driving Timing Chart

MODE = “VSS” (fCLK = 6.75MHz)

-Vertical Timing

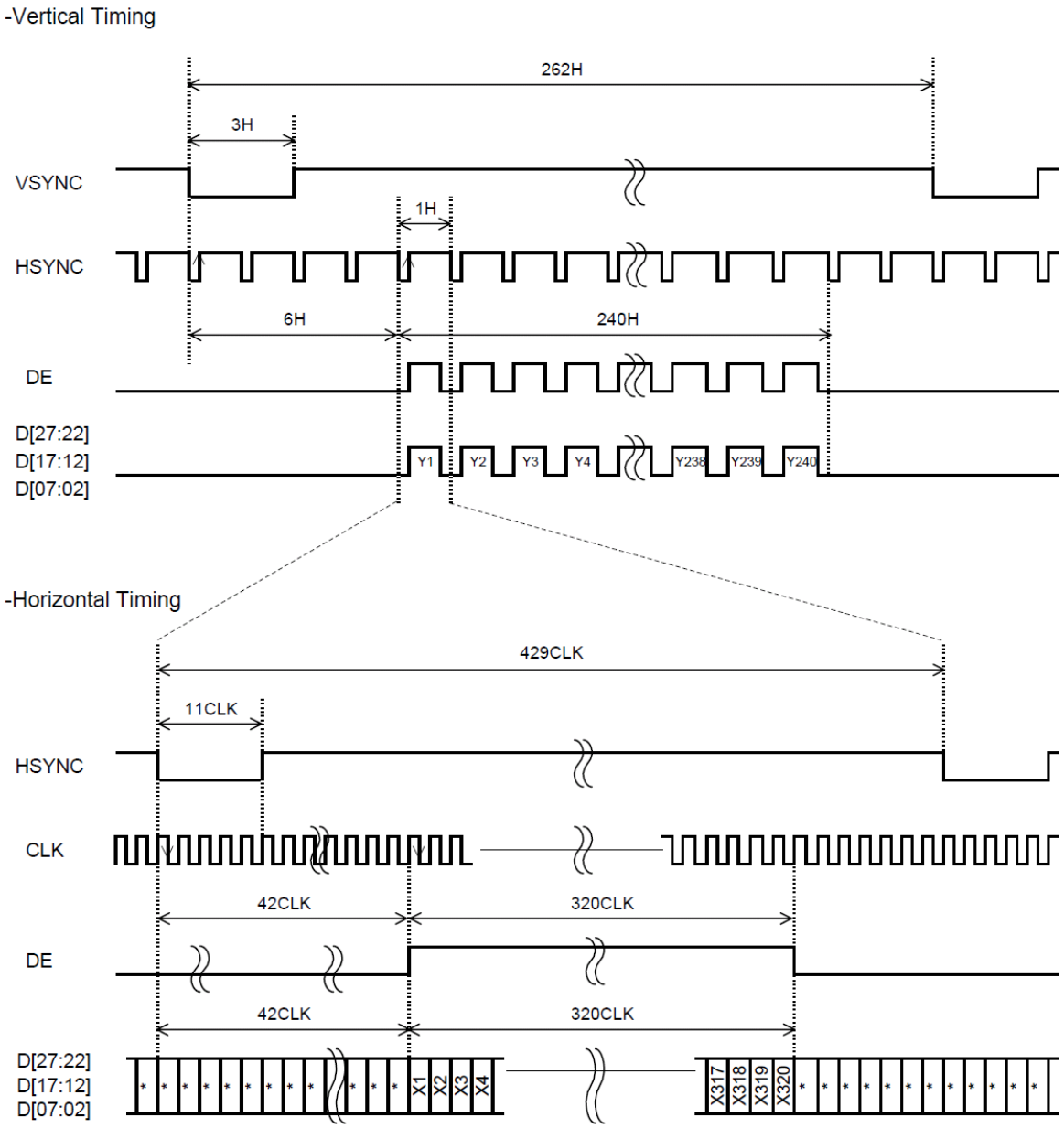


-Horizontal Timing



3.4.7 Example of Driving Timing Chart

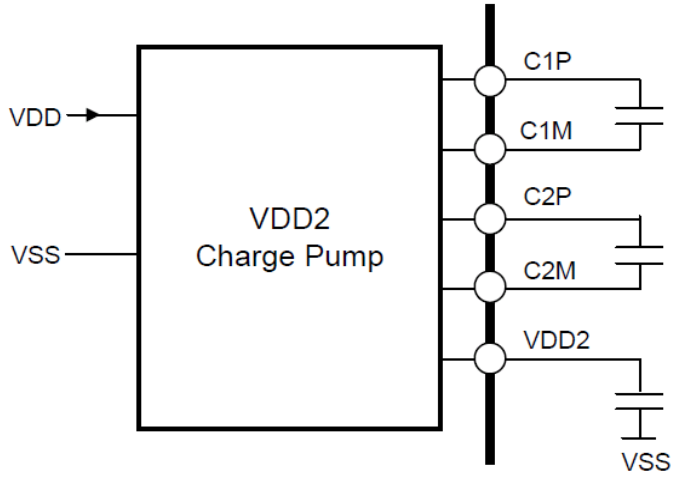
MODE = “VDD” (fCLK = 6.75MHz)



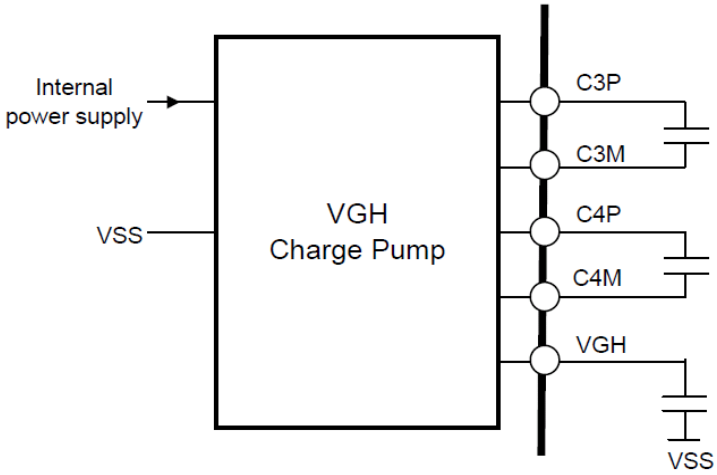
3.5 DESCRIPTION OF OPERATION

3.5.1 Power Supply

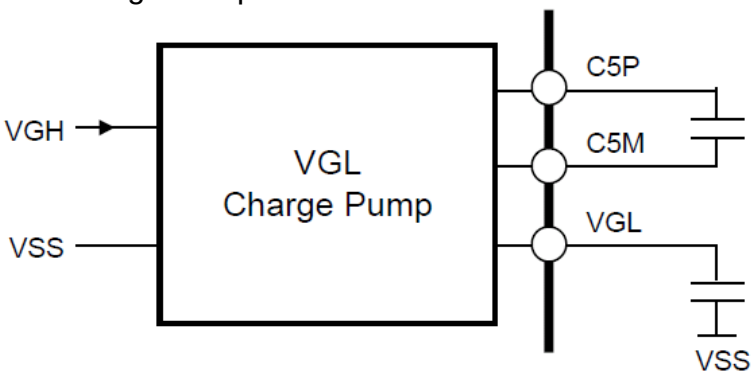
VDD2 Charge Pump



VGH Charge Pump



VGL Charge Pump

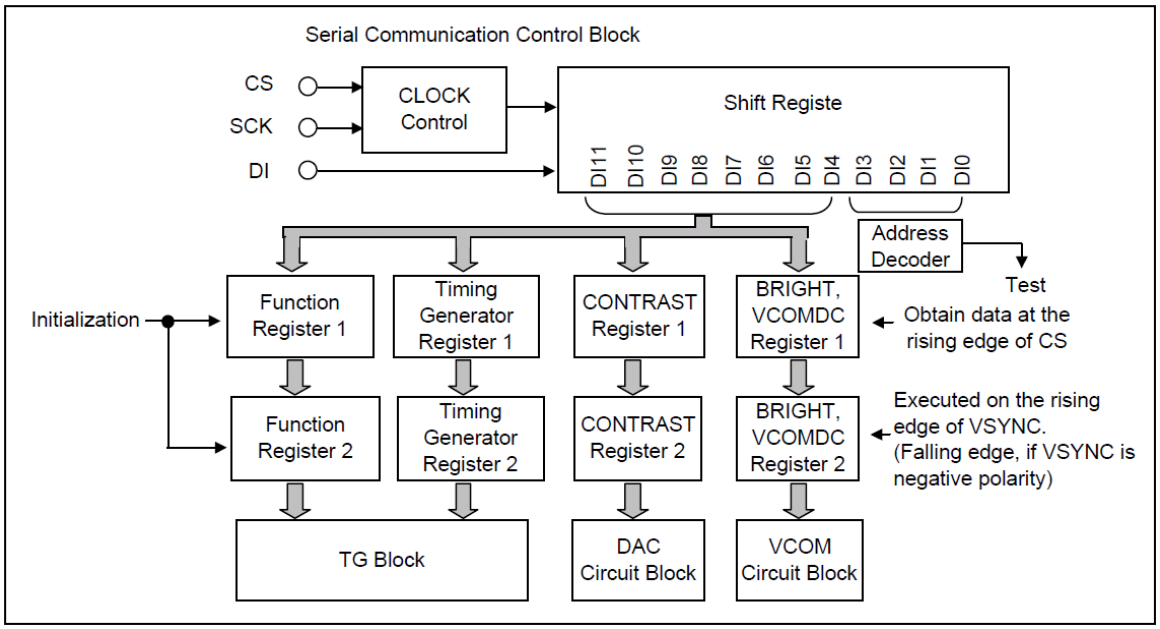


Please use ceramic capacitors with B property for external capacitors

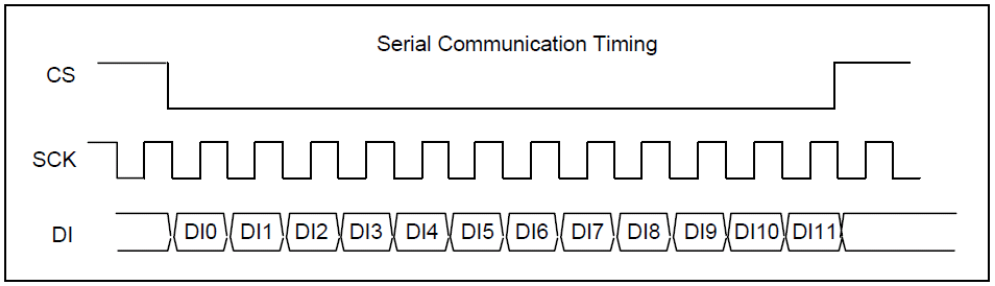
3.5.2 Serial Communication

Serial communication control function is effective at "MODE" = "VSS".

Feature Description
Serial communication control block is consist of registers that store data entered from CS, SCK, DI terminals and DAC that outputs control voltages to each part according to the data loaded from these registers .All registers are set to initial values at power-on. Electrostatics or noises may re-set the registers to improper values.
It is advisable to set up serial communication as frequently as possible as liquid crystal could degrade if such state is left untreated for a long time.



Serial Communication Timing
After input signal of CS drops from Hi to Lo, the Shift Resister loads 12 bits of serial data from DI at the rising edge of the input signal of SCK.
Mode register and DAC register load the stored data at the rising edge of the input signal of CS. When loaded DI data during the low period of CS is less than 12 bits, all loaded data are discarded.
When loaded DI data during the low period of CS is 12 bits or more, the last read of 12 bits is used .Each command is executed by VSYNC immediately after the rising the edge of CS.
Serial Communication Control Block is configurable at any time during display and standby mode as it is completely independent from other circuitry run by CLK in the monitor.



3.5.2.1Serial Communication Data

Configuration of serial data for DI terminal

First LSB											Last MSB
DI0	DI1	DI2	DI3	DI4	DI5	DI6	DI7	DI8	DI9	DI10	DI11
Register address				Data							

Register	Address				Number of bits for data	Preset value (LSB → MSB)								User setting value (LSB → MSB)							
	DI0	DI1	DI2	DI3		DI4	DI5	DI6	DI7	DI8	DI9	DI10	DI11	DI4	DI5	DI6	DI7	DI8	DI9	DI10	DI11
BRIGHT	0	0	0	0	6 (DI6-DI11)	-	-	0	1	0	1	1	0	-	-	User setting					
VCOMDC	1	0	0	0	6 (DI6-DI11)	-	-	1	1	1	1	1	1	-	-	Optimum setting for each monitor					
CONTRAST	0	1	0	0	4 (DI4-DI7)	0	1	1	1	-	-	-	-	User setting				-	-	-	-
PANEL1					3 (DI9-DI11)	-	-	-	-	-	0	0	1	-	-	-	-	-	0	0	1
VDISP	1	1	0	0	5 (DI4-DI8)	1	0	1	0	1	-	-	-	User setting				-	-	-	
PANEL2					3 (DI9-DI11)	-	-	-	-	-	0	0	0	-	-	-	-	-	0	0	0
HDISP	0	0	1	0	8 (DI4-DI11)	0	1	0	1	0	0	1	0	User setting							
PANEL3	1	0	1	0	8 (DI4-DI11)	0	1	0	0	1	1	0	0	0	1	0	0	1	1	0	0
FUNC1	0	1	1	0	8 (DI4-DI11)	0	0	0	1	0	0	0	0	0	User setting				0	0	0
FUNC2	1	1	1	0	8 (DI4-DI11)	1	1	1	1	0	0	0	0	User setting			1	0	0	-	-
FUNC3	0	0	0	1	8 (DI4-DI11)	0	0	0	0	0	0	0	0	0	0	User setting					
FUNC4	1	0	0	1	8 (DI4-DI11)	1	0	0	0	0	0	0	0	1	User setting						
PANEL4	0	1	0	1	8 (DI4-DI11)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PANEL5	1	1	0	1	8 (DI4-DI11)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
PANEL6	0	0	1	1	8 (DI4-DI11)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PANEL7	1	0	1	1	8 (DI4-DI11)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PANEL8	0	1	1	1	8 (DI4-DI11)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PANEL9	1	1	1	1	8 (DI4-DI11)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Configuration of FUNC1 Register

bit	Function	Description
DI4	TEST 0	Please fix it to "0".
DI5	Vertical flip display	Flip image vertically (from top to bottom). 0: Normal, 1: Vertical flip
DI6	Horizontal flip display	Flip image horizontally (from side to side). 0: Normal, 1: Horizontally flip
DI7	Backlight control	Set BLON signal that controls external backlight circuitry. 0: Low 1: High
DI8	Standby control	Switch between standby and operation. 0: standby, 1: operation
DI9	TEST 1	Please fix it to "0".
DI10	TEST 2	
DI11	TEST 3	

Configuration of FUNC2 Register

bit	Function	Description
DI4	HSYNC polarity	Change polarity of HSYNC. 0: Positive polarity, 1: Negative polarity
DI5	VSYNC polarity	Change polarity of VSYNC. 0: Positive polarity, 1: Negative polarity
DI6	CLK polarity	Change polarity of CLK. 0: Noninversion 1: Inversion
DI7	TEST 4	Please fix to "1".
DI8	TEST 5	Please fix it to "0".
DI9	TEST 6	
DI10	Unused	-
DI11	Unused	

Configuration of FUNC3 Register

bit	Function	Description
DI4	Test 7	Please fix it to "0".
DI5	Test 8	
DI6	GM1[0]	Register for gamma potential correction when input data D [*7:*0] is 192(=C0h).
DI7	GM1[1]	
DI8	GM1[2]	
DI9	GM2[0]	Register for gamma potential correction when input data D[*7:*0] is 148(=94h).
DI10	GM2[1]	
DI11	GM2[2]	

Configuration of FUNC4 Register

bit	Function	Description
DI4	Test 9	Please fix to "1".
DI5	Select gamma correction curve	Select gamma correction curves. 0: built-in gamma correction curve 1: user-established gamma correction curve
DI6	GM3[0]	Register for gamma potential correction when input data D [*7:*0] is 108(=6Ch).
DI7	GM3[1]	
DI8	GM3[2]	
DI9	GM4[0]	Register for gamma potential correction when input data D[*7:*0] is 64(=40h).
DI10	GM4[1]	
DI11	GM4[2]	

-TEST 0 to TEST 9

Please fix DI4, DI9 through DI11 of the FUNC1 registers to "0".
Please fix DI7 of FUNC2 to "1", DI8 and DI9 of FUNC2 to "0". DI10 and DI11 are no connection.
Please fix DI4 and DI5 of FUNC3 to "0".
Please fix DI4 of FUNC4 to"1".

-User Setting Values

Please use "User setting values" to set up PANEL1 through PANEL9, DI4, DI9 through DI11 of FUNC1, DI7 through DI9 of FUNC2, DI4, DI5 of FUNC3 and DI4 of FUNC4.
Use of unspecified values may cause malfunction

3.5.3 Detailed Description of Functions

(1) Bright Control (BRIGHT)

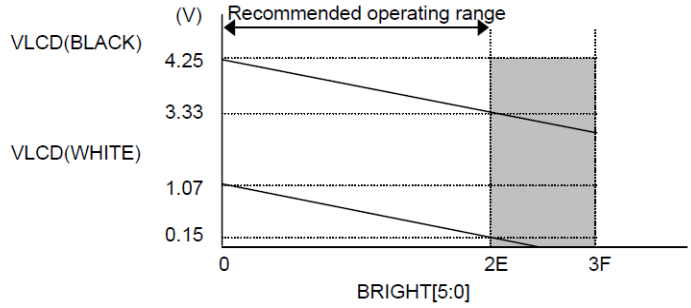
Bright setting values is controlled by 6 bit (DI6 through DI1) of BRIGHT registers. The display lightens in proportion to data value while VLCD changes inversely with the data value.
Initial value of BLACK[00h] is 3.73V and WHITE[FFh] is 0.55V when the CONTRAST register is Eh

The amount of change in VLDC is 0.02V per LSB

Recommended Operating Range
The register shall be set in 00h to E2h range

BRIGHT[5:0]	VLCD(BLACK)	VLCD(WHITE)
00h	4.25V	1.07V
01h	4.23V	1.05V
~	~	~
1Ah	3.73V	0.55V
~	~	~
2Dh	3.35V	0.17V
2Eh	3.33V	0.15V

Recommended operating range



(2) Common Electrode Center Voltage (VCOMDC)

Common-electrode center voltage is controlled by 6-bit (DI6 through DI11). The voltage is proportional to data values. Each TFT monitor has to be optimized to its own optimum value separately. This optimization is mandatory. If not implemented, liquid crystal of TFT monitor will be degraded by long operation. Initial value of VCOMDC is 2.30V.(Typ.)

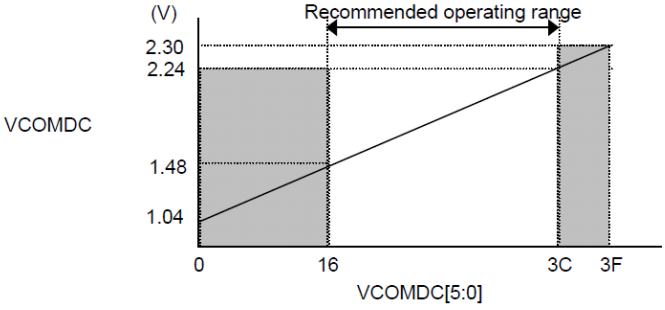
Amount of change in VCOMDC is 0.02V per LSB

Recommended Operating Range

Since VCOMDC has its optimum value somewhere between 1.48V and 2.24V, the register should be set in 16h to 3Ch range.

VCOMDC[5:0]	VCOMDC (V)
00h	1.04V
~	~
15h	1.46V
16h	1.48V
~	~
3Ch	2.24V
~	~
3Fh	2.30V

Recommended operating range



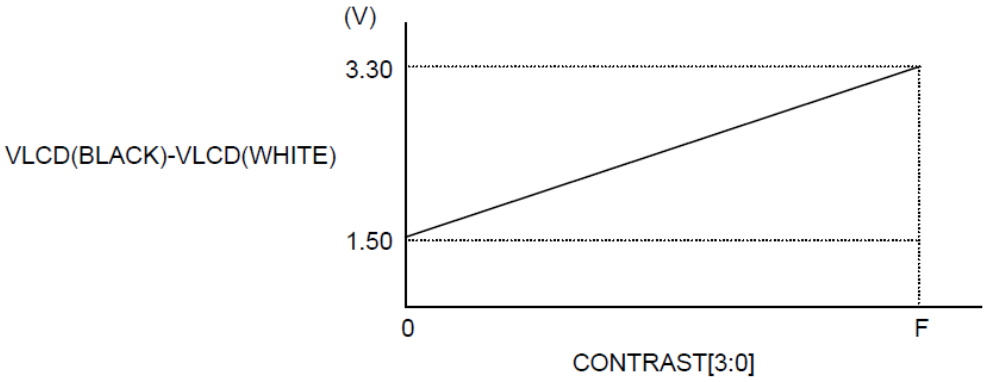
(3) Contrast Control (CONTRAST)

Contrast is controlled in 16 levels by 4-bit (DI4 through DI7) CONTRAST register.
Contrast is proportional to data values.
Contrast does not affect aforementioned bright control

Initial value of Contrast is 3.18V.Amount of change in contrast is 0.12V per LSB

(Typ.)

CONTRAST[3:0]	VLCD(BLACK)-VLCD(WHITE)
0h	1.50V
~	~
Eh	3.18V
Fh	3.30V



(4) Panel Setting 1 (PANEL 1)

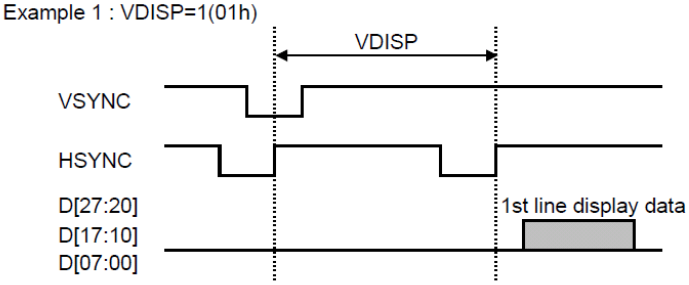
PANEL 1 register 3-bit (DI9 to DI11) can select operating conditions from 8 choices.
Please set this register to these values.

DI9	DI10	DI11
0	0	1

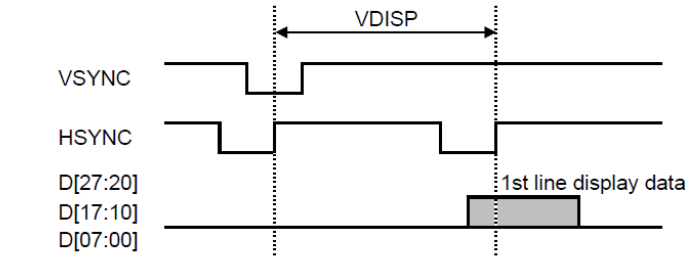
(5) Vertical Flyback Time Set (VDISP)

The length of vertical fly back period can be set from 0 to 31H by 5-bit of DI4 through DI8 of VDISP register. When VSYNC and HSYNC are negative polarity, "Lo" period of VSYNC is detected at the rising edge of HSYNC.
The setting value of VDISP is determined by the number of horizontal periods from the first detection of VSYNC=Lo to the first line's display data input. Please set VDISP=1 as shown in "Example 1" even if the display data of the first line is input
When the pulse width of VSYNC extends over two or more H as shown in "Example 3", the setting value is determined by the number of horizontal periods from the first detection of VSYNC=Lo to the first line's display data input.
When the initial value is "0", the first line's display data needs to be inputted immediately after VSYNC as shown in "Example 4".
When VDISP=0, please use odd number for the setting of the total number of lines that compose one field. This function can also be used for vertical display range setup (Vertical position setup).

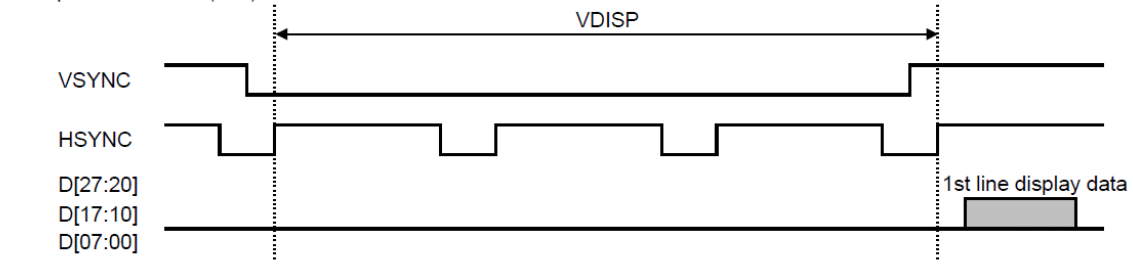
Example 1 : VDISP=1(01h)



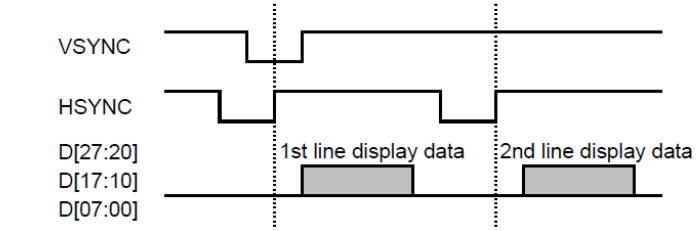
Example 2 : VDISP=1(01h)



Example 3 : VDISP=3(03h)



Example 4 : VDISP=0(00h)



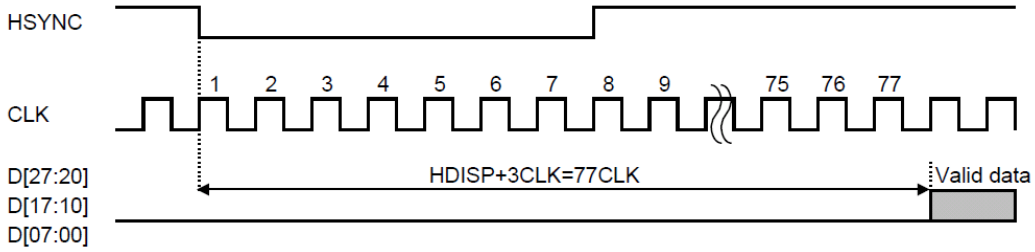
(6) Panel Setting 2 (PANEL2)

PANEL 2 register 3-bit (DI9 and DI11) can select operating conditions from 8 choices. Please set this register to these values:

DI9	DI10	DI11
0	0	0

(7) Horizontal Flyback Period Setting (HDISP)

Horizontal flyback time can be set from 5 to 258CLK by HDISP register with 8-bit of DI14 thru DI11. However, set value of 0 or 1 is prohibited. Actual flyback time is "setting value plus 3CLK". When initial value is 74, a data after a lapse of 74 + 3CLK=77CLK from the rising edge of HSYNC is displayed as shown in the following chart.
This function can also be used for horizontal display range setup (Horizontal position setup).
Example: HDISP=74(4Ah)



(8) Panel Setting 3 (PANEL3)

Select operating condition of the signal generated by driver IC in accordance with 8-bit of DI4 to DI11 of PANEL 3 register. Please set this register to these values.

DI4	DI5	DI6	DI7	DI8	DI9	DI10	DI11
0	1	0	0	1	1	0	0

(9) Function Set 1 (FUNC1)

FUNC1 register sets and controls the following functions by its each bit of DI5, DI6, DI7 and di8.

-Vertical Flip Display (Up/Down)
DI5=0 for normal display, DI5 =1 for vertical flip display
After completing the setup by serial communication, the selected display mode is carried out by VSYNC.
(Normal display is defined when FPC of the monitor is place downside.)

-Horizontal Flip Display (Right/Left)
DI6=0 for normal display, DI6=1 for horizontal flip display
The selected display mode is executed at VSYNC after setup by serial communication.

(Please refer to the section 3.5.4. for Display Data Transfer)

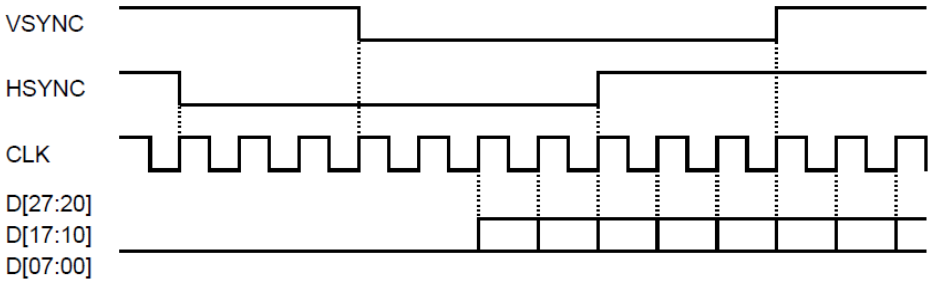
-Backlight Control
DI7 switches the backlight driver IC. BLON terminal outputs set value of DI7.
Since its output level is VDD or VSS, this function can also be used for other controls than the backlight.
After completing the setup by serial communication, the selected display mode is carried out by VSYNC.

-Standby Mode
DI8=0 for standby mode, DI8 =1 for normal operation
Since default value of DI8 after power on is "0", it automatically goes to standby mode. Power consumption is significantly reduced in standby mode by disabling the timing generator and the LCD driving circuitry, and disconnecting current lines.
No image is displayed (white raster display) during standby mode unless DI8 is set to 1 for normal operation by serial communication. Serial data can be received by serial communication block even in standby mode.
Please refer to the section 3.5.5. "Standby (Power save) Sequence" for standby mode and power on/off sequence.
When normal operation is switched to standby mode, afterimage treatment is carried out before switching to standby mode.

(10) Function Set 2 (FUNC2)

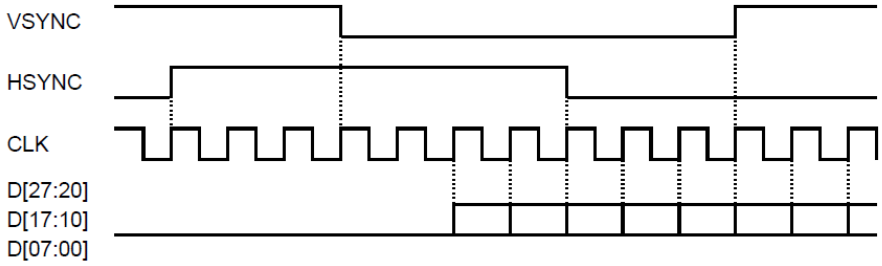
FUNC2 register sets and controls the following functions by its each bit of DI4 thru DI6.

-HSYNC, VSYNC, CLK Polarity Switching
Polarity of HSYNG is switched by DI4. DI4=0 for positive polarity input, DI4=1 for negative polarity input.
Polarity of VSYNC is switched by DI5. DI5=0 for positive polarity input, DI5=1 for negative polarity input.
Polarity of CLK is switched by DI6. DI6=0 for non-inversion, DI6=1 for inversion.
Initial value of DI4, DI5 and DI6 are "1". The following chart shows polarity of each signal at the initial value.
Please set change of VSYNC, HSYNC and display data at the rising edge of CLK.

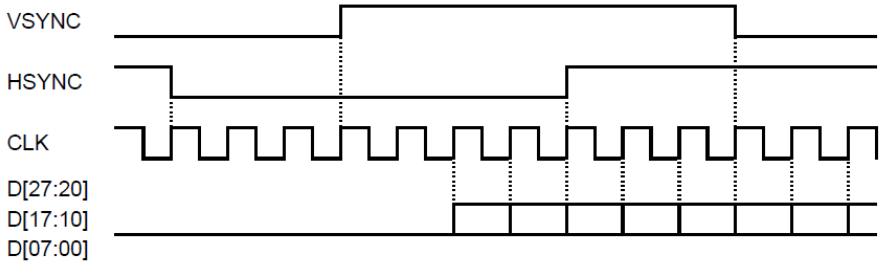


Polarity of each signal can be changed independently by logic of DI4, DI5 and DI6.

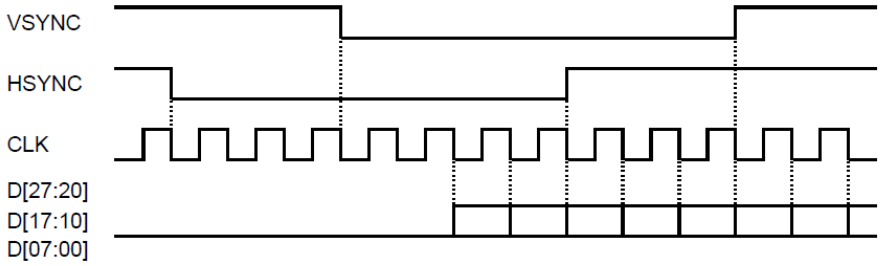
Example 1 : DI4=0,DI5=DI6=1 (HSYNC has positive polarity and Hi active)



Example 2 : DI4=1,DI5=0,DI6=1 (VSYNC has positive polarity and Hi active)



Example 3 : DI4=DI5=1,DI6=0 (CLK is reversed, data is read at the rising edge of CLK.)



(11) Function Set 3, 4 (FUNC 3, 4)

-Gamma Curve Correction Select

DI5=0 of FUNC 4 Register: Deactivate user configurable gamma correction circuitry. Use built-in gamma curve.
DI5=1 of FUNC 4 Register: Activate user configurable gamma correction circuitry. Use user configurable gamma correction curve.

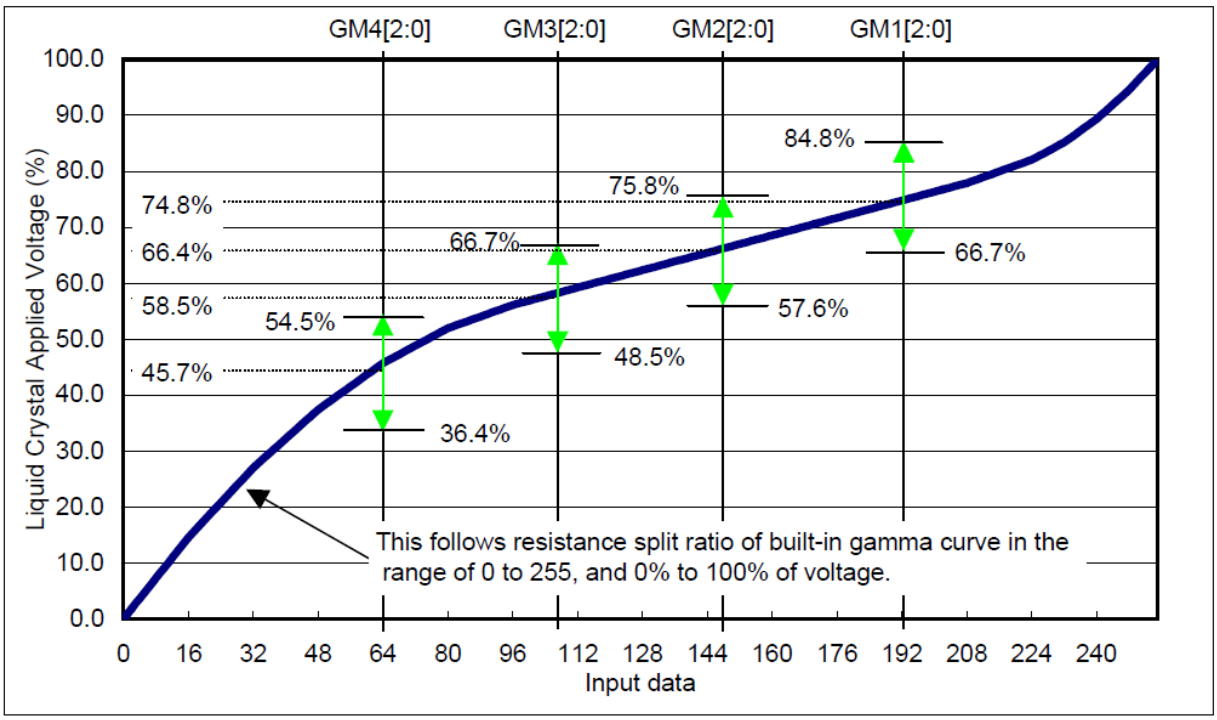
-Setting Method of User Configurable Gamma Correction Curve

Gamma curve can be corrected by using GM1[2:0] thru GM4[2:0] registers of FUNC 3 and FUNC 4.GM1 thru GM4 corrects each following gamma potential respectively.

GM1[2:0] → Input data D[*7:*0] = Register for gamma potential correction at 192(=C0h)
GM2[2:0] → Input data D[*7:*0] = Register for gamma potential correction at 148(=94h)
GM3[2:0] → Input data D[*7:*0] = Register for gamma potential correction at 108(=6Ch)
GM4[2:0] → Input data D[*7:*0] = Register for gamma potential correction at 64(=40h)

Below chart shows characteristic curve of grey scale input data - liquid crystal applied voltage. Input value of "0" is assumed to be 0% of applied voltage to liquid crystal, and input value of "225" is assumed to be 100% of applied voltage to liquid crystal. Adjustable range of GM1 thru GM4 registers are described below.

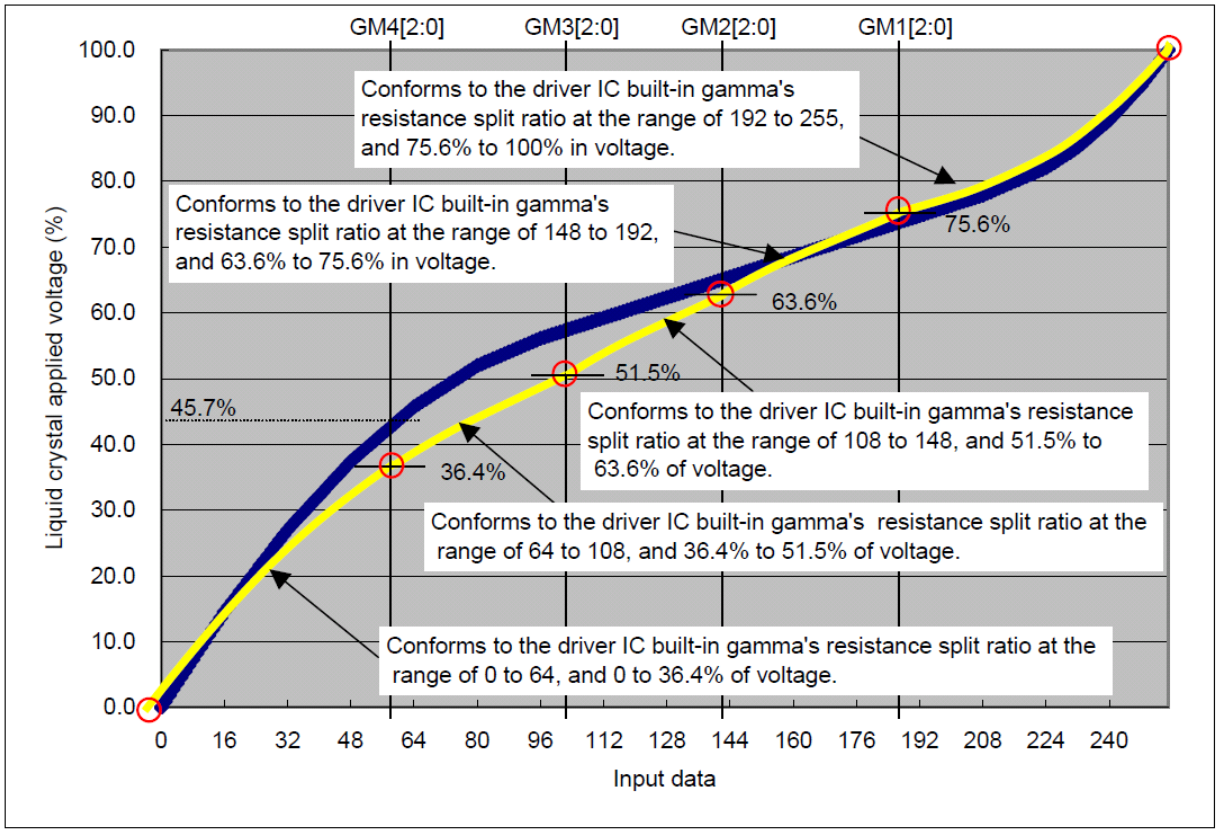
	GM4[2:0]	GM3[2:0]	GM2[2:0]	GM1[2:0]
00h	No correction	No correction	No correction	No correction
01h	54.5%	66.7%	75.8%	84.8%
02h	51.5%	63.6%	72.7%	81.8%
03h	48.5%	60.6%	69.7%	78.8%
04h	45.5%	57.6%	66.7%	75.6%
05h	42.4%	54.5%	63.6%	72.7%
06h	39.4%	51.5%	60.6%	69.7%
07h	36.4%	48.5%	57.6%	66.7%



When no correction is made to gamma potential of GM1 to GM4;
The voltages at "0" and "255" are fixed in accordance with the contrast and brightness settings, and voltages at 1 to 254 are determined by resister split ratio produced by the driver IC built-in gamma curve resister. (Refer to the chart in previous page)
Liquid crystal applied voltage takes the values of 45.7%, 58.5%, 66.4% and 74,8% when input date is 64, 108, 148 and 192 respectively.

When correction is made to any of GM1 to GM4 by user;
The voltage is corrected in accordance with a correction point and its set value configured by user. The voltages at 1 to 254 are determined by resister split ratio between voltage at 0 and 225 and input data.

Example: Darken grey scale in black side.
→ Change liquid crystal applied voltage at the 64 point to darken side.
→ Set GM4[2:0] to 7h, GM3[2:0] to 6h, GM2[2:0] to 5h and GM1[2:0] to 4h.



(12) Panel Select 4 (PANEL 4)

Select operating condition of the signal generated by driver IC in accordance with 8-bit of DI4 to DI11 of PANEL 4 register. Please set this register to this value.

DI4	DI5	DI6	DI7	DI8	DI9	DI10	DI11
0	0	0	0	0	0	0	0

(13) Panel Select 5 (PANEL 5)

Select operating condition of the signal generated by driver IC in accordance with 8-bit of DI4 to DI11 of PANEL 5 register. Please set this register to this value.

DI4	DI5	DI6	DI7	DI8	DI9	DI10	DI11
0	1	0	0	0	0	0	0

(14) Panel Select 6 (PANEL 6)

Select operating condition of the signal generated by driver IC in accordance with 8-bit of DI4 to DI11 of PANEL 6 register. Please set this register to this value.

DI4	DI5	DI6	DI7	DI8	DI9	DI10	DI11
0	0	0	0	0	0	0	0

(15) Panel Select 7 (PANEL 7)

Select operating condition of the signal generated by driver IC in accordance with 8-bit of DI4 to DI11 of PANEL 7 register. Please set this register to this value.

DI4	DI5	DI6	DI7	DI8	DI9	DI10	DI11
0	0	0	0	0	0	0	0

(16) Panel Select 8 (PANEL 8)

Select operating condition of the signal generated by driver IC in accordance with 8-bit of DI4 to DI11 of PANEL 8 register. Please set this register to this value.

DI4	DI5	DI6	DI7	DI8	DI9	DI10	DI11
0	0	0	0	0	0	0	0

(17) Panel Select 9 (PANEL 9)

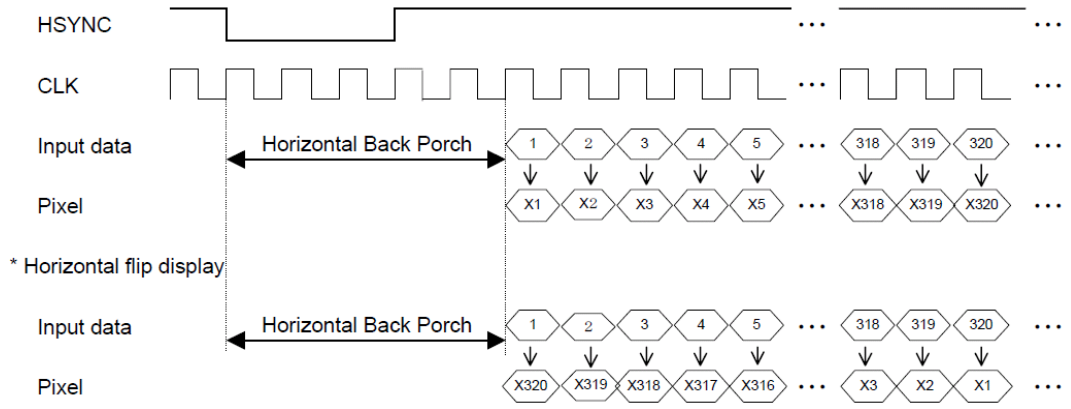
Select operating condition of the signal generated by driver IC in accordance with 8-bit of DI4 to DI11 of PANEL 9 register. Please set this register to this value.

DI4	DI5	DI6	DI7	DI8	DI9	DI10	DI11
0	0	0	0	0	0	1	0

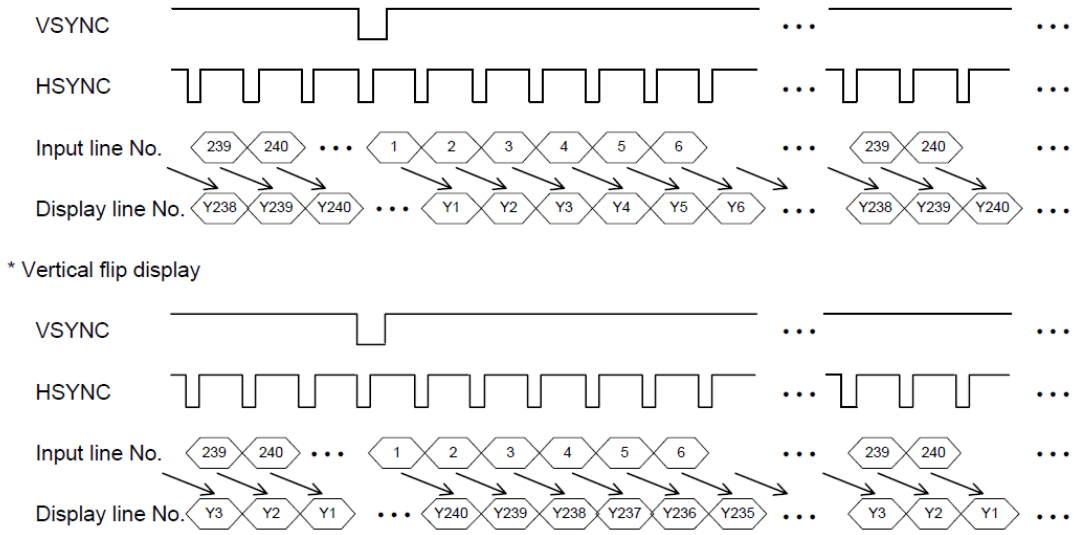
3.5.4 Display Data Transfer

Input display data to D[27:20],D[17:10],D[07:00]. D*0 : LSB, D*7 : MSB

-Horizontal Timing and Order of Input Data
Display data shall be input in synchronization with CLK.
Polarity of CLK can be selected by DI16 of FUNCTION SET 2 (FUNC2).(at "MODE" = "VSS")
Normal display: Normal display is defined as the orientation that the FPC cable on the TFT monitor is placed on the downside



-Vertical Timing and Order of Input Data
Transfer of display data that consist of 240 lines in 1 field is explained below. The correlations between input line and display line at normal display and vertical flip display are described below.
Normal display: Normal display is defined as the orientation that the FPC cable on the TFT monitor is placed on the downside.



* Above timing charts show correlation between input data and pixels in visual way and it is not actual timing chart.

3.5.5 Standby (Power Save) Sequence

When "MODE" = "VSS", serial communication signals of CS, DI and SCK shall be input after VDD stabilizes at VDD≧[0.9×VDD]V for more than 20 msec or more after power on.
All initial values of serial data shall be set during this standby mode.
Other logic input signals of HSYNC,VSYNC,D[27:20],D[17:10],D[07:00] and CLK shall be input simultaneously after power on (specified period marked ① in next page). All input signals shall be set to a fixed DC to reduce power consumption during standby mode.

Please follow the recommended power on/off sequence described below.

① Right after power on, serial communication registers are initialized. Therefore, standby control bit takes the value of "0". By this procedure the LCD goes into standby mode which significantly reduces power consumption of the LCD.
No image is displayed (white raster display) on the screen and internal power circuit is deactivated during standby mode.
Sync signal and display data (HSYNC,VSYNC,D[27:20],D[17:10],D[07:00],CLK) start to input before standby mode is released by serial communication.

② When the standby control bit is set to "1" by serial communication or the terminal "STBY" turn to "Lo" from "Hi", the standby mode is released by following VSYNC and the power supply circuit of building into begins operating.
No image is displayed (white raster display) on the screen for 5 fields from the following VSYNC after the release of standby mode.

③ LCD goes into normal display (display under normal operation) at the timing of VSYNC after completion of the procedure described in ②. Backlight shall be lit up 1 or more field after going to normal display.

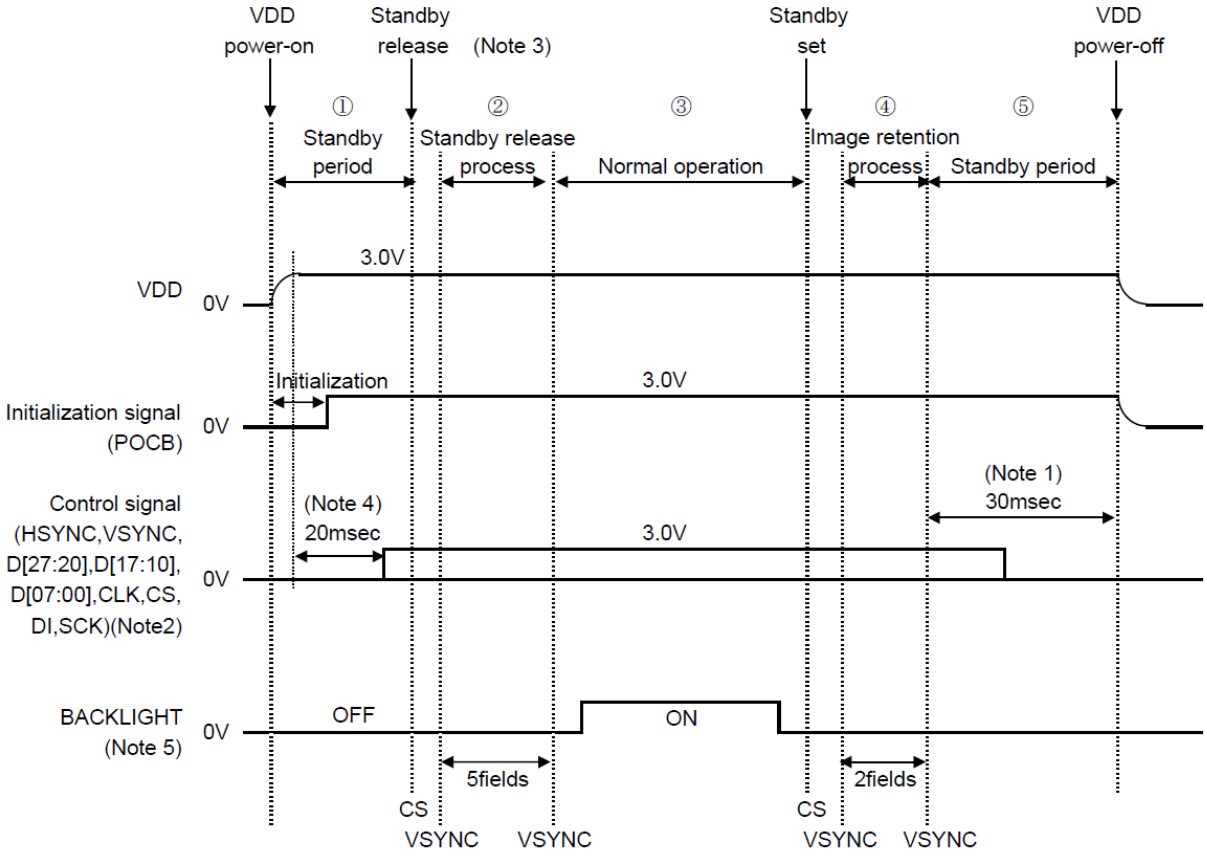
④ Standby mode can be established by setting standby control bit to "0" by serial communication or the terminal "STBY" turn to "Hi" from "Lo".
Display data is changed to FFh at VSYNC that comes right after this serial communication, and afterimage treatment is performed for 2 fields of VSYNC. Displayed image under normal display is immediately changed to white raster display by this treatment.
Continue to input sync signal （HSYNC,VSYNC,CLK) during this period.

⑤ LCD goes into standby mode, which is same as ① above, at the timing of VSYNC after completion of the procedure described in ④. Serial communication data is retained during standby mode. Serial communication signal and input signal can be deactivated.

② to ④ repeats same procedures as described above.

Below procedure must be followed for power-off.

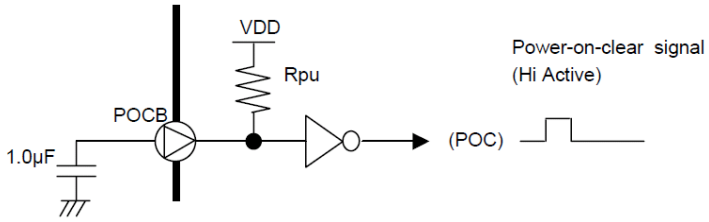
① Implement standby setting.
② After standby setting, continue to input sync signals (HSYNC, VSYNC, CLK) during the image treatment period (until VSYNC after 2 fields subsequent to standby setting).
③ After ②, power off VDD after 30msec or more.
④ Stop the sync signals (HSYNC, VSYNC, CLK) subsequent to afterimage treatment period and no later than VDD off.



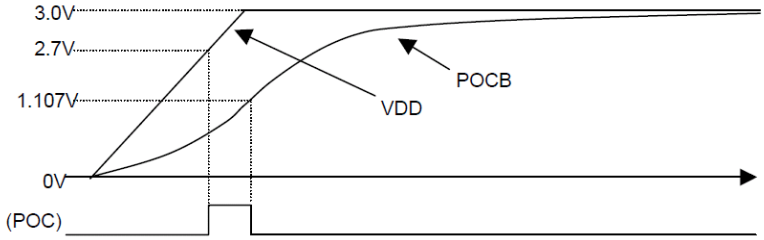
Note 1:Power off VDD more than 30 msec after VSYNC that arrives 2 fields from standby set.
Note 2:Input CLK during the period of inputting sync signals (HSYNC, VSYNC) and display data D[27:20],D[17:10],D[07:00].
Note 3:Due consideration needs to be given to power supply capacity as bigger current (inrush current) flows at standby release.
Note 4:Serial communication signals should be input after VDD stabilizes at VDD≧[0.9×VDD]V for more than 20 msec. And initial values of all serial data should be set during this period before standby release.
Note 5:Backlight should be turned on after 5 fields from starting display. Backlight should be turned off before standby is set. Voltage values shown in this chart are typical values, not fixed values.

3.5.6 POWER ON SEQUENCE

There is the following limit between a power on period and the serial communication setting.
Power-on-clear circuit diagram

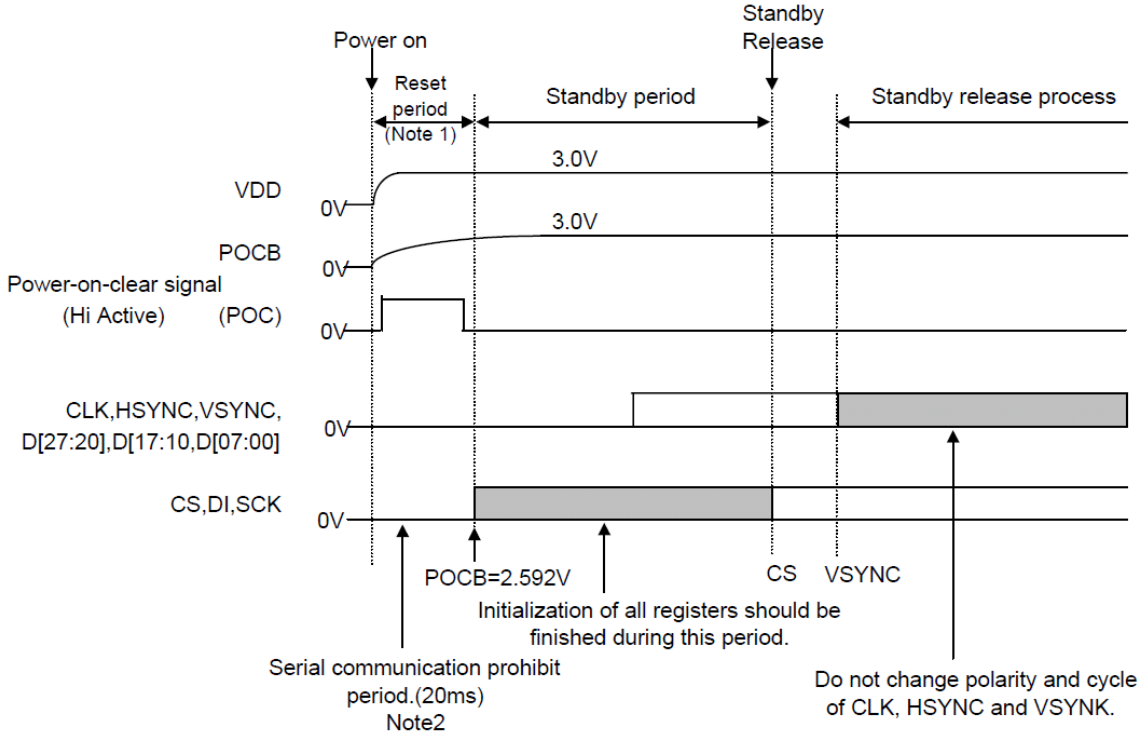


FPOCB terminal is connected to VDD through the pull-up resistor (Rpu).
When rising of VDD takes long time, POCB will have unstable and unpredictable waveform.
Please determine value of external capacitor by which POCB takes 1.107 V or less at VDD is 2.7V.



Power On Sequence

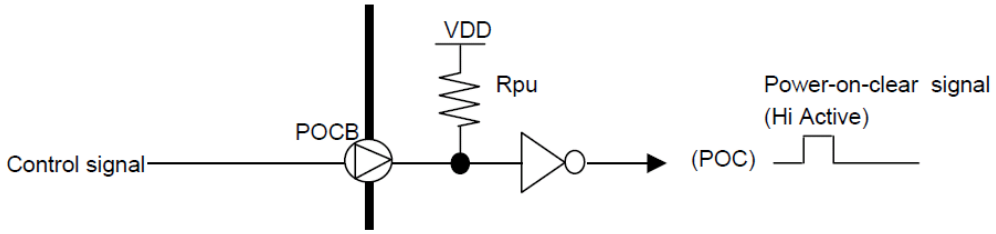
Serial Communication Prohibition Period



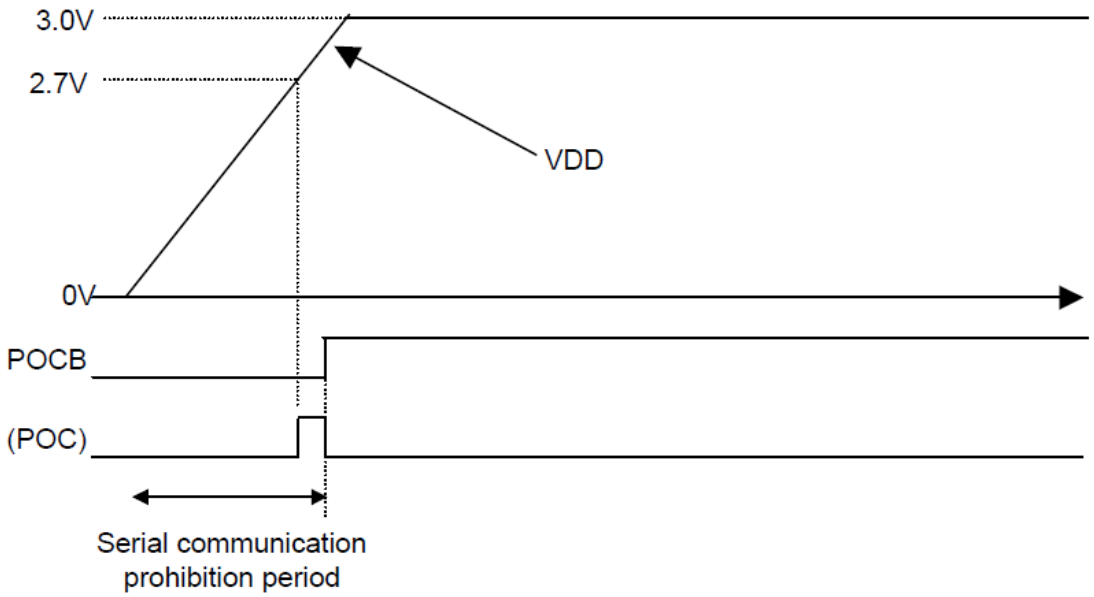
Note 1 All logic input signals are ignored during input period (POC is Hi).
Note 2: Serial communication signals shall be input after VDD stabilizes at VDD≧[0.9×VDD]V for more than 20 msec or more after power on.

In case of rapid startup after power-on, directly control POCB terminal.

Power-on-clear circuit diagram



In case of directly controlling POCB terminal, POCB terminal should be set to "Lo" at Power-on POCB should be changed to "Hi" after VDD is exceeding 2.7V.Serial communication is prohibited while POCB is "Lo".



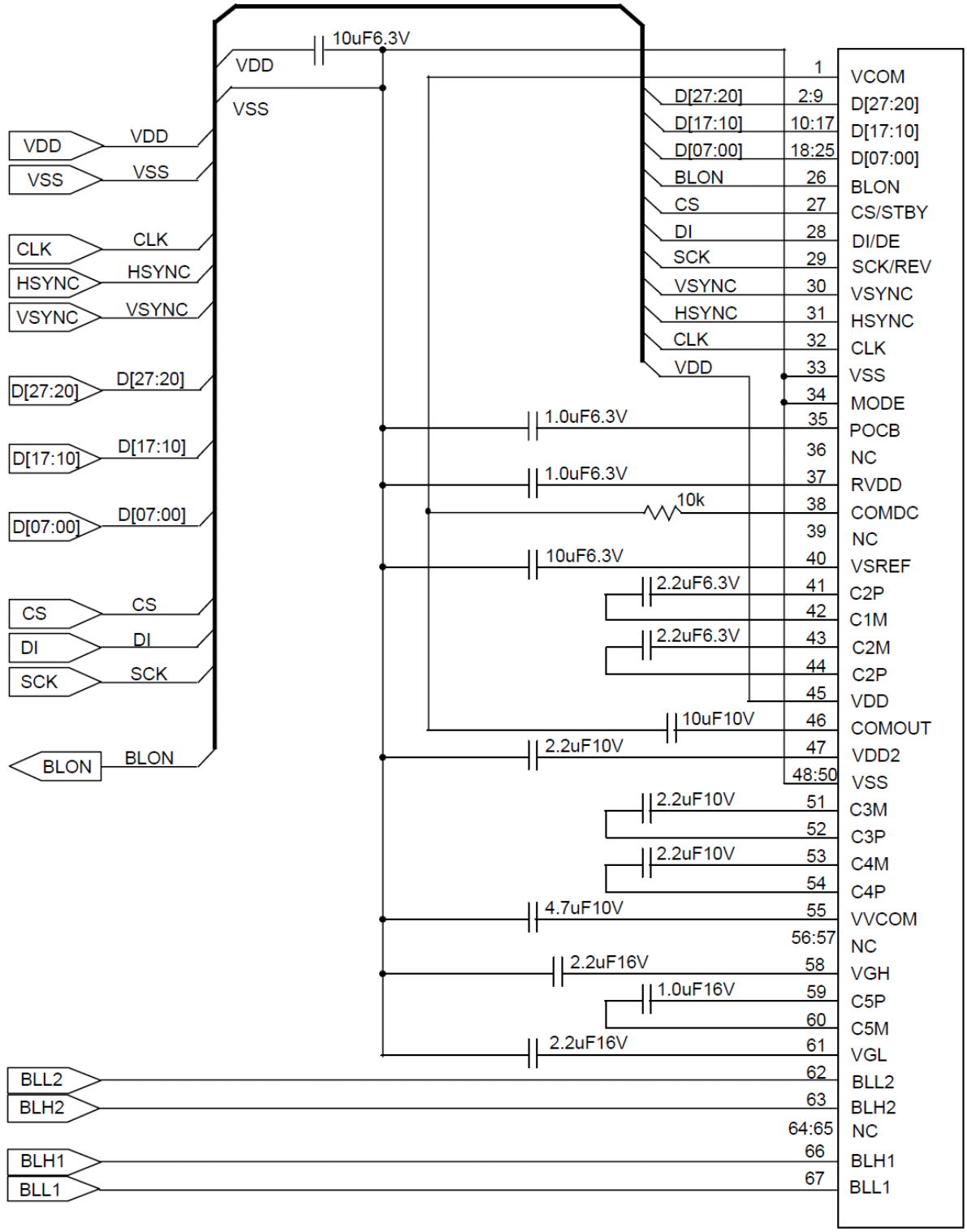
3.5.7 Other Functions

Built-in Panel Residual Charge Reduction Circuit

When the power turns off in accordance with the mandatory procedure described in the section "3.5.5. Standby (Power save) Sequence", afterimage treatment is carried out after standby mode is set. This circuit automatically reduces panel's residual charge and prevents afterimage for a long time even if standby mode setting fails to be made before power-off.

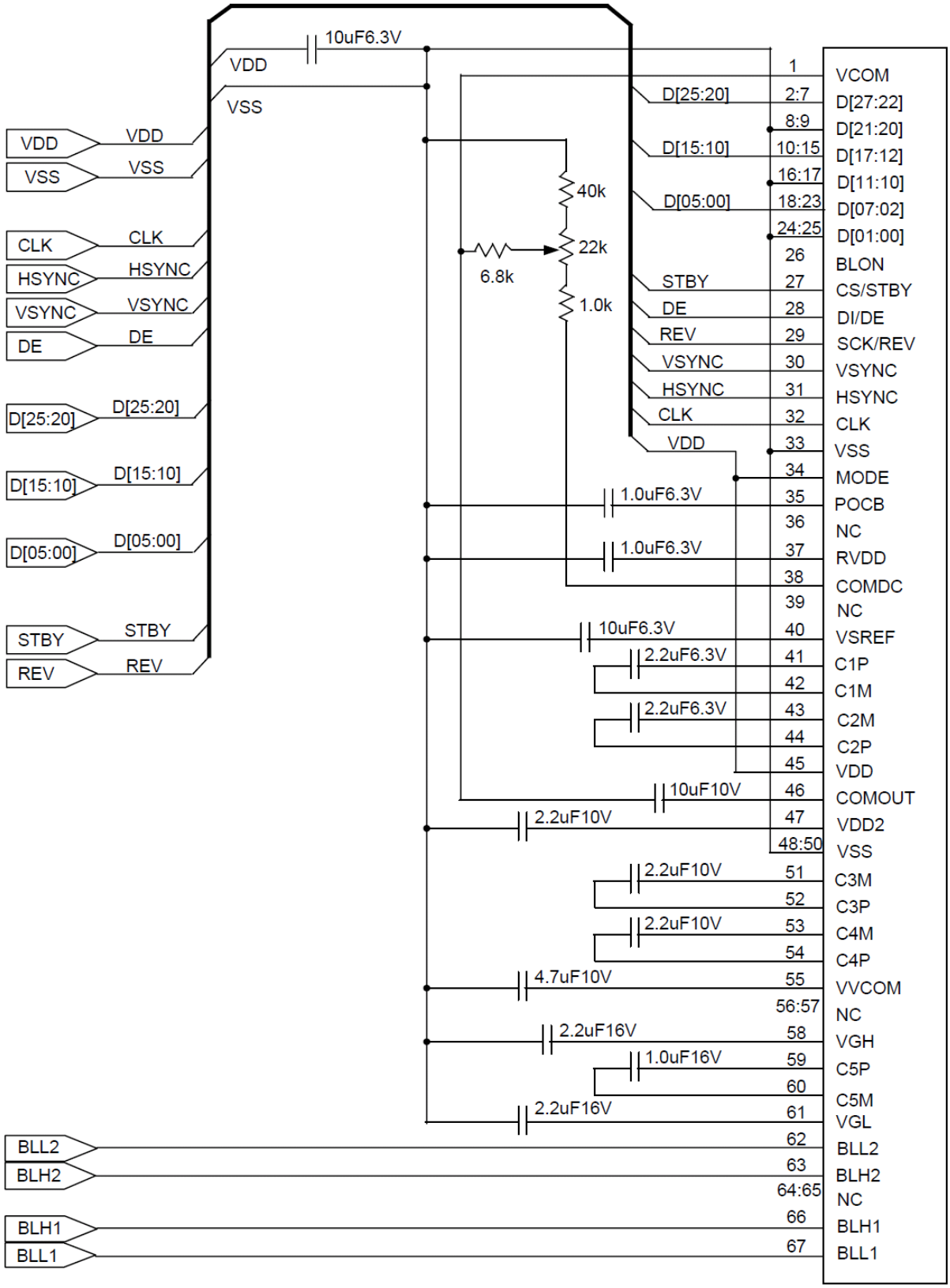
3.6 CIRCUIT

3.6.1 Driving circuit example (Module) [“MODE” = “VSS”]



TFT LCD MODULE REFERENCE CIRCUIT
This circuit is solely for reference purpose and optimum circuit and components values may be different. User's due consideration and evaluation must be given to this circuit design and component values prior to their intended use

3.6.2 Driving circuit example (Module) [“MODE” = “VDD”]



TFT LCD MODULE REFERENCE CIRCUIT

This circuit is solely for reference purpose and optimum circuit and components values may be different. User's due consideration and evaluation must be given to this circuit design and component values prior to their intended use

4 OPTICAL SPECIFICATION

4.1 OPTICAL CHARACTERISTICS

Ta = 25 °C

Item		Symbol	Condition	MIN	TYP	MAX	Unit	Note No.	Note
Response Time	Rise Time.	TON	VLCD= 0.69V→3.87V	-	-	40	ms	1	*
	Fall Time	TOFF	VLCD= 3.87V→0.69V	-	-	60	ms		
Contrast Ratio	Backlight ON	CR	VLCD= 0.69V/3.87V	240	400	-		2	
	Backlight OFF			-	9.0	-			
Viewing Angle	Left	θL	VLCD= 0.69V/3.87V CR ≥ 10	80	-	-	deg	3	*
	Right	θR		80	-	-	deg		
	Up	φU		80	-	-	deg		
	Down	φD		80	-	-	deg		
V-T Threshold Voltage		V90		0.7	1.0	1.3	V	4	*
		V50		1.2	1.5	1.8	V		
		V10		1.7	2.0	2.3	V		
White V-T Curve		-	-	White V-T Curve					Reference
White Chromaticity		x	VLCD= 0.69V	White Chromaticity Range				5	
		y							
Burn-in				No noticeable burn-in image should be observed after 2hours of window pattern display.				6	
Centre Brightness			VLCD= 0.69V	210	300	-	cd/m²	7	
Brightness Distribution			VLCD= 0.69V	70	-	-	%	8	

* <Measured in the form of LCD module.

<Measurement Condition>

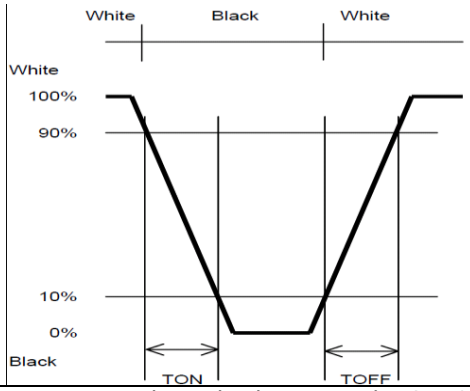
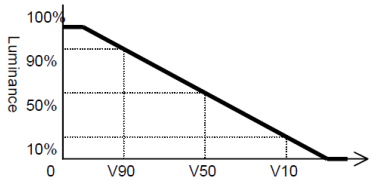
Measuring instruments: CS1000 (KONICA MINOLTA), LCD7000 OTSUKA ELECTRONICS), EZcontrast160D (ELDIM)

Driving condition: VDD= 3.0V, VSS= 0V
Optimized Vcom/c
VLCD= | Vsigpp±Vcompp | /2

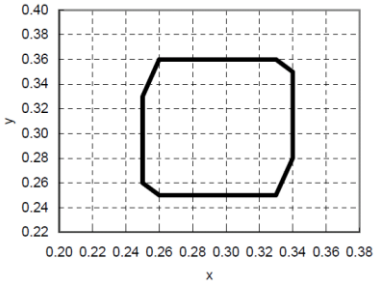
Backlight: IL=10mA

Measured temperature: Ta=25°C

4.1.1 Test Method

Note	Item	Test method	Measuring instrument	Remark
1	Response time	Measure output signal waveform by the luminance meter when raster of window pattern is changed from white to black and from black to white.  	LCD7000	Black display VLCD=3.87V White display VLCD=0.69V TON Rise Time TOFF Fall Time
2	Contrast ratio	Measure maximum luminance Y1 (VLCD=0.69V) and minimum luminance Y2 (VLCD=3.87V) at the centre of the screen by displaying raster or window pattern. Then calculate the ratio between these two values. Contrast ratio = Y1/Y2 Diameter of measuring point: 8mmφ	CS1000 LCD7000	Backlight ON Backlight OFF
3	Viewing angle Horizontal θ Vertical φ	Move the luminance meter from right to left and up and down and determinate the angles where contrast ratio is 10	EZcontrast160D	
4	V-T Threshold Value	Change VLCD by 0.1V step and plot the points where the luminance is 90% as V90, 50% as V50 and 10% as V10 of maximum luminance.  	LCD7000	
5	White chromaticity	Measure chromaticity coordinates x and y of CIE1931 colorimetric system at VLCD=0.69V Colour matching faction: 2° view	CS1000	
6	Burn-in	Visually check burn-in image on the screen after 2 hours of “window display” (VLCD=0.69V/3.87V).		At optimized VCOMDC
7	Centre brightness	Measure the brightness at the centre of the screen	CS1000	
8	Brightness distribution	(Brightness distribution)= 100 x B/A % A: max. brightness of the 9 points B: min. brightness of the 9 points	CS1000	

【White Chromaticity Range】



x	y
0.25	0.33
0.25	0.26
0.26	0.25
0.33	0.25
0.34	0.28
0.34	0.35
0.33	0.36
0.26	0.36

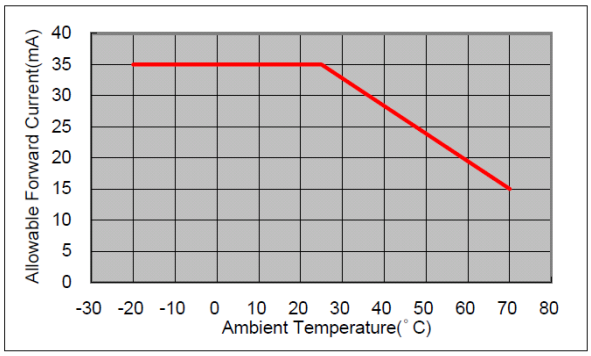
5 BACKLIGHT SPECIFICATION

5.1 LED DRIVING CONDITIONS

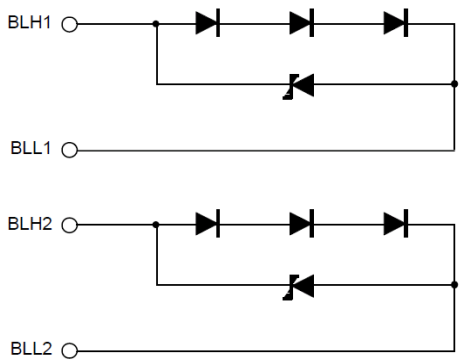
Item	Symbol	Condition	Rating			Unit	Applicable Terminal
			Min	Typ	Max		
Forward Current	IL25	Ta= 25°C	-	10.0	35.0	mA	BLH1-BLL1 BLH2-BLL2
	IL70	Ta= 70°C	-	-	15.0	mA	
Forward Voltage	VL	Ta= 25°C, IL= 10.0 mA	-	9.0	9.9	V	
Estimated Life of LED	LL	Ta= 25°C, IL= 10.0 mA Note	-	(50,000)	-	hr	

Note:

- The lifetime of the LED is defined as a period till the brightness of the LED decreases to the half of its initial value.
- This figure is given as a reference purpose only, and not a guarantee.
- This figure is estimated for an LED operating alone.
  As the performance of an LED may differ when assembled as a monitor together with a TFT panel due to different environmental temperature.
- Estimated lifetime could vary on a different temperature and usually higher temperature could reduce the life significantly.



5.2 LED CIRCUIT



6 QUALITY ASSURANCE SPECIFICATION

6.1 DEFECTIVE DISPLAY AND SCREEN QUALITY

Observed TFT-LCD monitor from front during operation with the following conditions

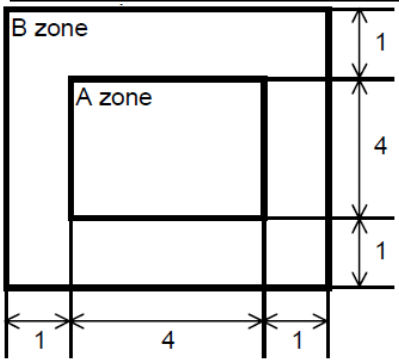
Driving signal	Raster Pattern (RGB in monochrome, white black)
Signal condition	VLCD: 0.69V, 1.65 V, 3.87V (3 Steps)
Observation Distance	30cm
Illuminance	200 to 350 lx
Backlight	IL= 10mA

Defect item		Defect content		Criteria
Display Quality	Line defect	Black, white or color line, 3 or more neighboring defective dots		Not exists
	Dot defect	Uneven brightness on dot-by-dot base due to defective TFT or CF, or dust is counted as dot defect (brighter dot, darker dot) High bright dot: Visible through 2% ND filter at VLCD=3.87V Low bright dot: Visible through 5% ND filter at VLCD=3.87V Dark dot: Appear dark through white display at VLCD=1.65V		Refer to table 1
Screen Quality	Dirt	Point-like uneven brightness (white stain, black stain etc)		Invisible through 1% ND filter
	Foreign particle	Point-like	0.25mm<φ	N=0
			0.20<φ≦0.25mm	N≦2
			φ≦0.20mm	Ignored
		Liner	3.0mm<length and 0.08mm<width	N=0
			length≦3.0mm or width≦0.08mm	Ignored
	Others			Use boundary sample for judgment when necessary

φ(mm): Average diameter = (major axis + minor axis)/2
Permissible number: N

Table 1

Area	High bright dot	Low bright dot	Dark dot	Total	Criteria
A	0	2	2	3	Permissible distance between same color bright dots (includes neighboring dots): 3 mm or more
B	2	4	4	6	Permissible distance between same color high bright dots (includes neighboring dots): 5 mm or more
Total	2	4	4	7	



Division of A and B areas
B area: Active area
Dimensional ratio between A and B areas: 1: 4: 1 (Refer to the left figure)

6.2 SCREEN AND OTHER APPEARANCE

Testing conditions
Illuminance 1200~2000 lx
Observation distance 30cm

Item		Criteria	Remark
Polarizer	Flaw Stain Bubble Dust Dent	Ignore invisible defect when the backlight is on.	Applicable area: Active area only
S-case		No functional defect occurs	
FPC cable		No functional defect occurs	

6.3 DEALING WITH CUSTOMER COMPLAINTS

6.3.1 Non-conforming analysis

Purchaser should supply Densitron with detailed data of non-conforming sample. After accepting it, Densitron should complete the analysis in two weeks from receiving the sample.
If the analysis cannot be completed on time, Densitron must inform the purchaser.

6.3.2 Handling of non-conforming displays

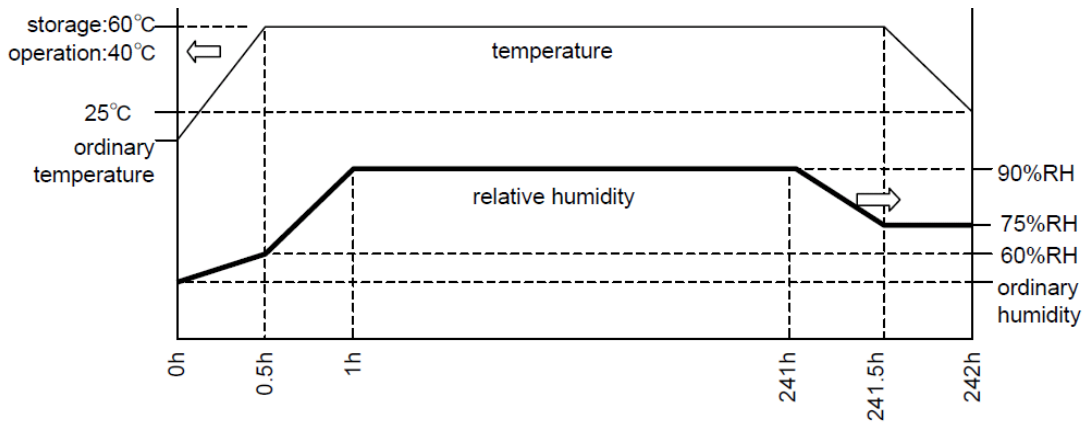
If any non-conforming displays are found during customer acceptance inspection which Densitron is clearly responsible for, return them to Densitron.
Both Densitron and customer should analyse the reason and discuss the handling of non-conforming displays when the reason is not clear.
Equally, both sides should discuss and come to agreement for issues pertaining to modification of Densitron quality assurance standard.

7 RELIABILITY SPECIFICATION

7.1 RELIABILITY TESTS

Test Item		Test Condition	Number of failures/ number of examinations
Durability Test	High Temperature Storage	Ta= 80˚C 240h	0/3
	Low Temperature Storage	Ta=-30˚C 240h	0/3
	High Temperature & High Humidity Storage	Ta= 60°C, RH= 90% Non condensing 240h	0/3
	High Temperature Operation	Tp= 70°C 240h	0/3
	Low Temperature Operation	Tp= -20°C 240h	0/3
	High Temperature & Humidity Operation	Tp= 40°C RH= 90% 240h Non condensing	0/3
	Thermal Shock Storage	-30←→ 80°C (30 min/ 30min) 100cycles	0/3
Mechanical Environmental Test	Electrostatic Discharge Test (non operation)	Confirms to EIAJ ED-4701/300 C= 200 pF, R= 0 Ω, V= ±200V Each 3 times of discharge on and power supply and other terminals.	0/3
	Surface Discharge Test (non operation)	C= 250 pF, R= 100 Ω, V=± 12kV Each 5 times of discharge in both polarities on the centre of screen with the case grounded.	0/3
	FPC tension test	Pull the FPC with the force of 3N for 10 seconds in the direction -90° to its original direction	0/3
	FPC bend test	Pull the FPC with the force of 3N for 10 seconds in the direction -180° to its original direction. Repeat 3 times	0/3
	Vibration test	Total amplitude 1.5 mm, f= 10~55 Hz, X,Y,Z directions for each 2 hours.	0/3
	Impact test	Use original jig and make an impact with peak acceleration of 1000 m/s²for 6 ms with half sine-curve at 3 times to each X, Y, Z directions in conformance with JIS 60068-2-27-1995	0/3
Packing Test	Packing Vibration-Proof Test	Acceleration of 19.6 m/s ² with frequency of 10 → 55→ 10 Hz, X, Y, Z direction for each 30 minutes.	0/1 Packing
	Packing Drop Test	Drop from 75 cm high. 1 time to each 6 surfaces, 3 edges, 1 corner	0/1 Packing

Note: Ta=ambient temperature Tp= Panel temperature



Reliability Criteria: measure following parameters after leaving the TFT at 25°C for 2 hours or more.

Item	Standard	Remark
Display quality	No visible abnormalities shall be seen	As per Quality Assurance Specification
Contrast ratio	40 or more	Backlight ON

8 HANDLING PRECAUTIONS

Safety
If the LCD panel breaks, be careful not to get the liquid crystal fluid in your mouth or in your eyes.
If the liquid crystal touches your skin or clothes, wash it off immediately using soap and plenty of water.

Mounting and Design
Place a transparent plate (e.g. acrylic, polycarbonate or glass) on the display surface to protect the display from external pressure. Leave a small gap between the transparent plate and the display surface.
When assembling with a zebra connector, clean the surface of the pads with alcohol and keep the surrounding air very clean.
Design the system so that no input signal is given unless the power supply voltage is applied.

Caution during LCD cleaning
Lightly wipe the display surface with a soft cloth soaked with Isopropyl alcohol, Ethyl alcohol or Trichlorotriflorothane.
Do not wipe the display surface with dry or hard materials that will damage the polariser surface.
Do not use aromatic solvents (toluene and xylene), or ketonic solvents (ketone and acetone).

Caution against static charge
As the display uses C-MOS LSI drivers, connect any unused input terminal to VDD or VSS.
Do not input any signals before power is turned on. Also, ground your body, work/assembly table and assembly equipment to protect against static electricity.

Packaging
Displays use LCD elements, and must be treated as such. Avoid strong shock and drop from a height.
To prevent displays from degradation, do not operate or store them exposed directly to sunshine or high temperature/humidity.

Caution during operation
It is indispensable to drive the display within the specified voltage limit since excessive voltage shortens its life. Direct current causes an electrochemical reaction with remarkable deterioration of the display quality. Give careful consideration to prevent direct current during ON/OFF timing and during operation. Response time is extremely delayed at temperatures lower than the operating temperature range while, at high temperatures, displays become dark. However, this phenomenon is reversible and does not mean a malfunction or a display that has been permanently damaged. If the display area is pushed on hard during operation, some graphics will be abnormally displayed but returns to a normal condition after turning off the display once. Even a small amount of condensation on the contact pads (terminals) can cause an electro-chemical reaction which causes missing rows and columns. Give careful attention to avoid condensation.

Storage
Store the display in a dark place where the temperature is 25°C ± 10°C and the humidity below 50%RH.Store the display in a clean environment, free from dust, organic solvents and corrosive gases.
Do not crash, shake or jolt the display (including accessories).