OLED DISPLAY MODULE

Product Specification

CUSTOMER	**Standard**	
PRODUCT NUMBER	**DD-12864YW-13A**	
CUSTOMER APPROVAL		**Date**

INTERNAL APPROVALS		
Product Mgr	Doc. Control	Electr. Eng
Bazile Peter	**Bazile Peter**	**Alan Wang**
Date: 16/04/13	Date: 16/04/13	Date: 16/04/13

☐ **Approval for Specification only**

☐ **Approval for Specification and Sample**

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REVISION RECORD

Rev.	Date	Page	Chapt.	Comment	ECR no.
A	16/04/13	--	--	Initial Release	

1 MAIN FEATURES

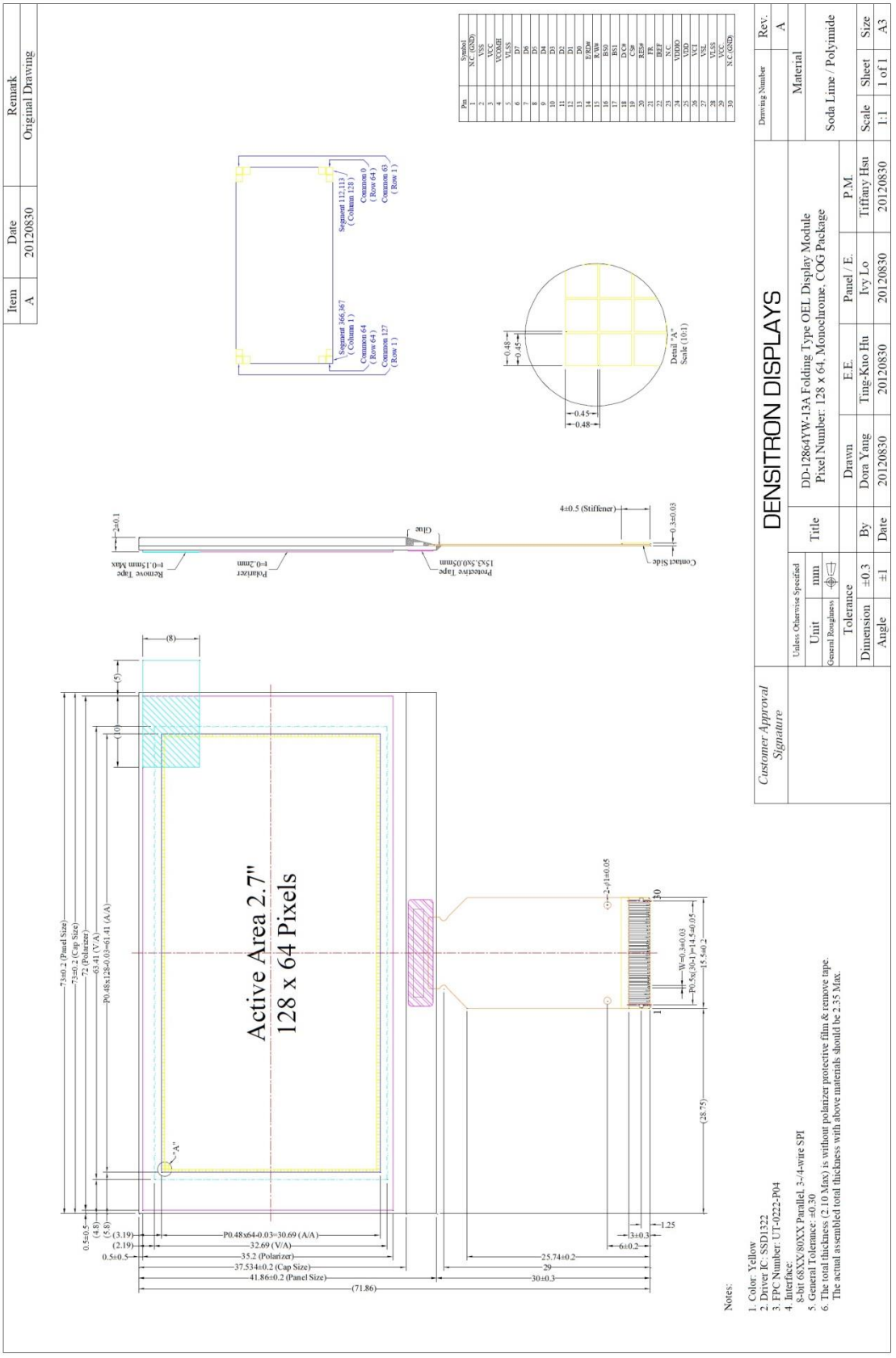
ITEM	CONTENTS
Display Format	128 x 64 Dots
Colour	Yellow Monochrome
Overall Dimensions	73.00 (W) × 41.86 (H) × 2.00 (D) mm
Viewing Area	63.41 (W) x 32.69 (H)
Screen Size	2.7”
Mode	Passive Matrix
Duty ratio	1/64
Driver IC	SSD1322
Operating temperature	-40°C ~ +70°C
Storage temperature	-40°C ~ +85°C

2 MECHANICAL SPECIFICATION

2.1 MECHANICAL CHARACTERISTICS

ITEM	CHARACTERISTIC	UNIT
Display Format	128 x 64	Dots
Overall Dimensions	73.00 (W) × 41.86 (H) × 2.00 (D)	mm
Viewing Area	63.41 (W) x 32.69 (H)	mm
Active Area	61.41 (W) x 30.69 (H)	mm
Dot Size	0.45 (W) 0.45 (H)	mm
Dot Pitch	0.48 (W) x 0.48 (H)	mm
Weight	12.17	g
IC Controller/Driver	SSD1322	

2.2 MECHANICAL DRAWING



3 ELECTRICAL SPECIFICATION

3.1 ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min	Max	Unit	Note
Supply Voltage for Operation	V_{CI}	-0.3	4	V	1, 2
Supply Voltage for Logic	V_{DD}	-0.5	2.75	V	1, 2
Supply Voltage for I/O pins	V_{DDIO}	-0.5	V_{CI}	V	1, 2
Supply Voltage for Display	V_{CC}	-0.5	16	V	1, 2
Operating Temperature	T_{OP}	-40	+70	℃	3
Storage Temperature	T_{STG}	-40	+85	℃	3
Static Electricity	Be sure that you are grounded when handling displays.				

Note 1: All the above voltages are on the basis of "VSS = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3.2 "Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80°C.

3.2 ELECTRICAL CHARACTERISTICS

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage for Operation	V_{CI}		V_{DD}	2.8	3.5	V
Supply Voltage for Logic	V_{DD}		2.4	2.5	2.6	V
Supply Voltage for I/O Pins	V_{DDIO}		1.65	-	V_{CI}	V
Supply Voltage for Display	V_{CC}	Note 4	14.5	15	15.5	V
High Level Input	V_{IH}	I_{OUT}=100µA	0.8xV_{DDIO}	--	V_{DDIO}	V
Low Level Input	V_{IL}	I_{OUT}=100µA	0	--	0.2xV_{DDIO}	V
High Level Output	V_{OH}	I_{OUT}=100µA	0.9xV_{DDIO}	--	V_{DDIO}	V
Low Level Output	V_{OL}	I_{OUT}=100µA	0	--	0.1xV_{DDIO}	V
Operating Current for V_{CI}	I_{CI}		-	0.18	0.3	mA
Operating Current for V_{CC}	I_{CC}	Note 5	-	17.8	22.3	mA
		Note 6	-	27.7	34.6	mA
		Note 7	-	47.3	59.1	mA
Sleep Mode Current for V_{CI}	$I_{CI,SLEEP}$		-	1	10	µA
Sleep Mode Current for V_{CC}	$I_{CC,SLEEP}$		-	4	20	µA

Note 4: Brightness (L_{br}) and Supply Voltage for Display (V_{CC}) are subject to the change of panel characteristics and the customer's request.

Note 5: V_{CI} = 2.8V, V_{CC} = 15V, 30% Display Area Turn on.

Note 6: V_{CI} = 2.8V, V_{CC} = 15V, 50% Display Area Turn on.

Note 7: V_{CI} = 2.8V, V_{CC} = 15V, 100% Display Area Turn on.

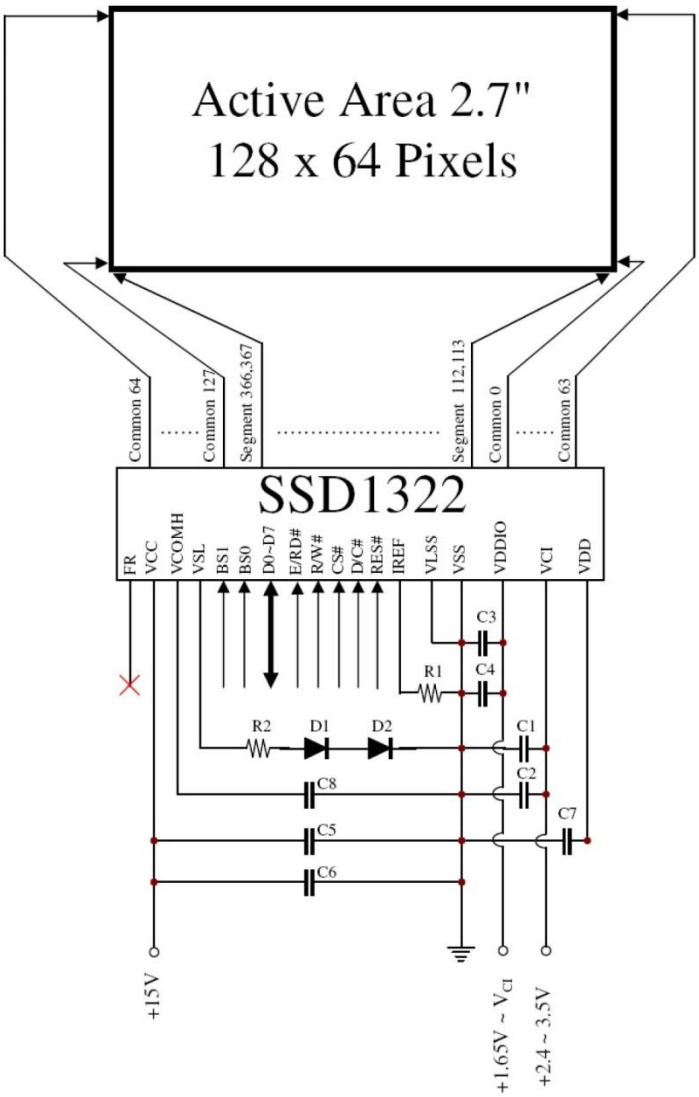
3.3 INTERFACE PIN ASSIGNMENT

<table>
<tr><th>No.</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>1</td><td>N.C. (GND)</td><td>--</td><td>Reserved Pin (Supporting Pin).
The supporting pins can reduce the influences from stresses on the function pins. This pin must be connected to external ground.</td></tr>
<tr><td>2</td><td>VSS</td><td>P</td><td>Ground of Logic Circuit
This is a ground pin. It also acts as a reference for the logic pins. It must be connected to external ground</td></tr>
<tr><td>3</td><td>VCC</td><td>P</td><td>Power Supply for OEL Panel
This is the most positive supply pin of the chip. They must be connected to external source.</td></tr>
<tr><td>4</td><td>VCOMH</td><td>P</td><td>Voltage Output High Level for COM Signal
This pin is the input pin for the voltage output high level for COM signals. A tantalum capacitor should be connected between this pin and VSS.</td></tr>
<tr><td>5</td><td>VLSS</td><td>P</td><td>Ground of Analog Circuit
This is analog ground pin. It should be connected to VSS externally</td></tr>
<tr><td>6~13</td><td>D7~D0</td><td>I/O</td><td>Host Data Input/Output Bus
These pins are 8-bit bi-directional data bus to be connected to the microprocessors data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK.
Unused pins must be connected to VSS except for D2 in serial mode.</td></tr>
<tr><td>14</td><td>E/RD#</td><td>I</td><td>Read/Write Enable or Read
This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low.
When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is low and CS# is pulled low.
When serial mode is selected, this pin must be connected to VSS.</td></tr>
<tr><td>15</td><td>R/W#</td><td>I</td><td>Read/Write Select or Write
This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to “High” for read mode and pull it “Low” for write mode.
When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low.
When serial mode is selected, this pin must be connected to VSS.</td></tr>
<tr><td>16
17</td><td>BS0
BS1</td><td>I</td><td>Communicating Protocol Select
These pins are MCU interface selection input. See the following table:
<table>
<tr><th></th><th>BS0</th><th>BS1</th></tr>
<tr><td>3-wire SPI</td><td>1</td><td>0</td></tr>
<tr><td>4-wire SPI</td><td>0</td><td>0</td></tr>
<tr><td>8-bit 68XX Parallel</td><td>1</td><td>1</td></tr>
<tr><td>8-bit 80XX Parallel</td><td>0</td><td>1</td></tr>
</table></td></tr>
</table>

18	D/C#	I	*Data/Command Control* This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 is treated as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register. When the pin is pulled high and serial interface mode is selected, the data at SDIN is treated as data. When it is pulled low, the data at SDIN will be transferred to the command register. When 3-wire Serial interface mode is selected, this pin must be connected to VSS. For detailed relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams
19	CS#	I	*Chip Select* This pin is the chip select input. When the pin is enabled for MCU communication only when CS# is pulled low.
20	RES#	I	*Power Reset for Controller and Driver* This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation.
21	FR	O	*Cascade Application Connection Pin* This pin is No Connection pins. Nothing should be connected to this pin. It should be left open individually.
22	IREF	I	*Current Reference for Brightness Adjustment* This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current at 10µA maximum.
23	N.C.	-	*Reserved Pin* The N.C. pin between function pins are reserved for compatible and flexible design.
24	VDDIO	P	*Power Supply for I/O Pin* This pin is a power supply pin of I/O buffer. It should be connected to VCI or external source. All I/O signals should have VIH reference to VDDIO. When I/O signals pins (BS0~BS1, D0~D7, control signals…) pull high, they should be connected to VDDIO.
25	VDD	P	*Power Supply for Core Logic Circuit* This is a voltage supply pin. It can be supplied externally (within the range of 2.4~2.6V) or regulated internally from VCI. A capacitor should be connected between this pin & VSS under all circumstances.
26	VCI	P	*Power Supply for Low voltage circuit* This is a voltage supply pin. It must be connected to external source & always be equal or higher than VDD & VDDIO.
27	VSL	P	*Voltage Output Low Level for SEG Signal* This is segment voltage reference pin. When external VSL is not used, this pin should be left open. When external VSL is used, this pin should connect with resistor and diode to ground.
28	VLSS	P	*Ground of Analog Circuit* This is the analog ground pin. It should be connected to VSS externally.
29	VCC	I	*Power Supply for OEL Panel* This is the most positive supply pin of the chip. This must be connected to external source.
30	N.C. (GND)	-	*Reserved Pin (Supporting Pin).* The supporting pins can reduce the influences from stresses on the

			function pins. This pin must be connected to external ground.

3.4 BLOCK DIAGRAM



C1, C3, C5: 0.1µF
C2, C4: 4.7µF
C6: 20µF
C7: 1µF
C8: 4.7uF / 25V Tantalum Capacitor
R1 = 910kΩ, R1= (Voltage at IREF – VSS) / IREF
R2: 50Ω, 1/4W
D1, D2: 0.7V, 0.5W

* FR should be left float.

MCU Interface Selection: Base on BS0 and BS1 connection
Pins connected to MCU interface: D7~D0, E/RD#, R/W#, D/C#, CS#, and RES#
Showed as below table:

BS1	BS0	Interface mode	Data bus								Control bus				
			D7	D6	D5	D4	D3	D2	D1	D0	CS#	D/C#	R/W#	E/RD#	RES#
0	0	4-wire SPI	**0**	**0**	**0**	**0**	**0**	**NC**	SDIN	SCLK	CS#	D/C#	**0**	**0**	RES#
0	1	3-wire SPI	**0**	**0**	**0**	**0**	**0**	**NC**	SDIN	SCLK	CS#	**0**	**0**	**0**	RES#
1	0	8bit 8080	D7	D6	D5	D4	D3	D2	D1	D0	CS#	D/C#	WR#	RD#	RES#
1	1	8bit 6800	D7	D6	D5	D4	D3	D2	D1	D0	CS#	D/C#	R/W#	E	RES#

Note:

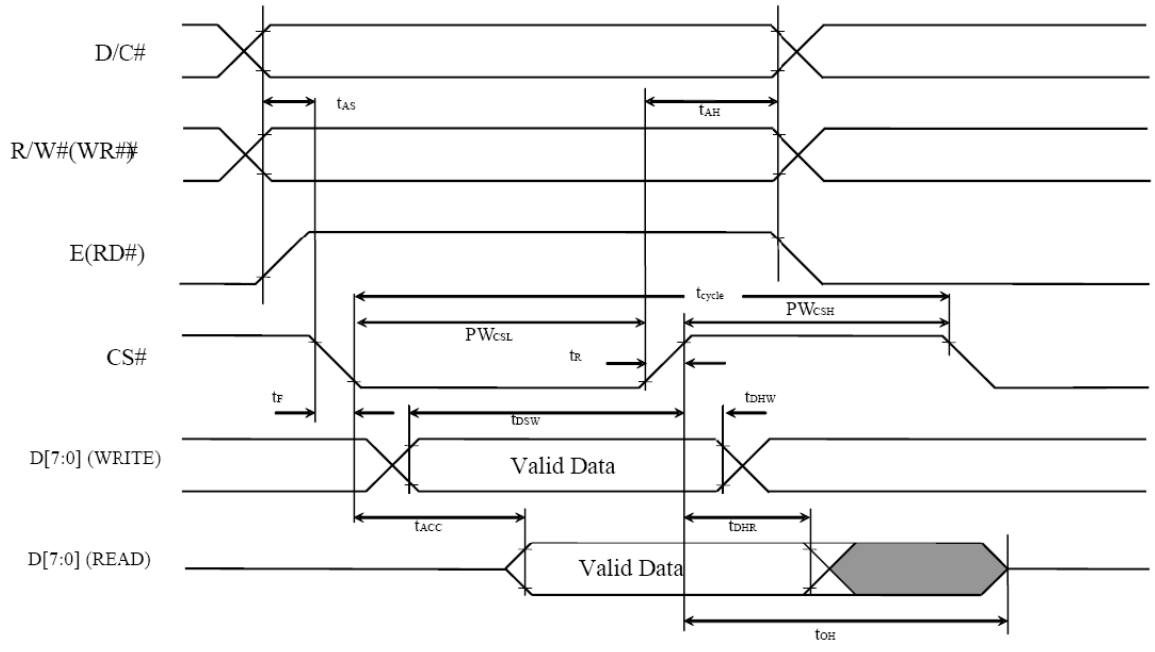
a. “0” is connected to VSS.
b. “1” is connected to VDD.
c. “NC” is non-connected.

3.5 TIMING CHARACTERISTICS

3.5.1 68XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	10	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (Read) Chip Select Low Pulse Width (Write)	120 60	-	ns
PW_{CSH}	Chip Select High Pulse Width (Read) Chip Select High Pulse Width (Write)	60 60	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

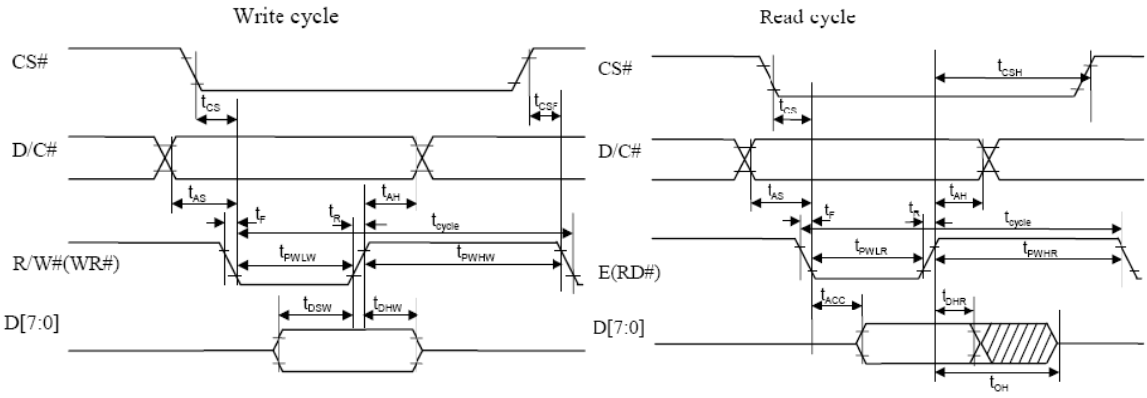
(V_{DD}-V_{SS} = 2.4V to 2.6V, V_{DDIO} = 1.65V, V_{CI} = 3.3V, T_a = 25℃)



3.5.2 80XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	10	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
t_{PWLR}	Read Low Time	150	-	ns
t_{PWLW}	Write Low Time	60	-	ns
t_{PWHR}	Read High Time	60	-	ns
t_{PWHW}	Write High Time	60	-	ns
t_{CS}	Chip Select Setup Time	0	-	ns
t_{CSH}	Chip Select Hold Time to Read Signal	0	-	ns
t_{CSF}	Chip Select Hold Time	20	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

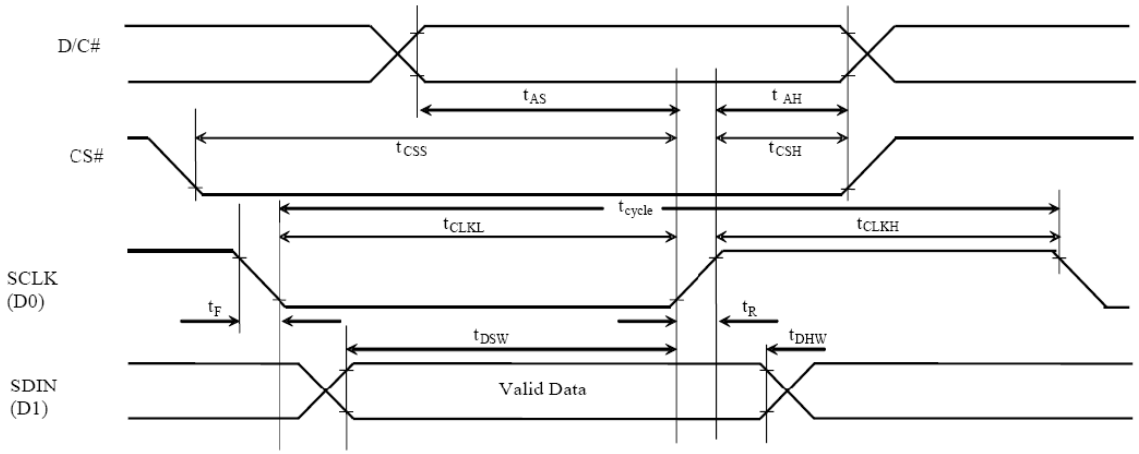
(V_{DD}-V_{SS} = 2.4V to 2.6V, V_{DDIO} = 1.65V, V_{CI} = 3.3V, T_a = 25℃)

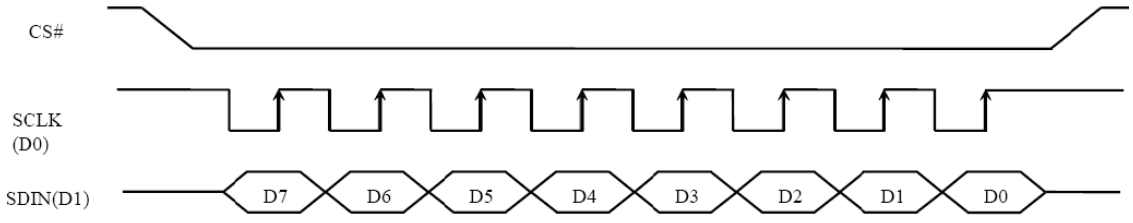


3.5.3 Serial Interface Timing Characteristics: (4-wire SPI)

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	ns
t_{AS}	Address Setup Time	15	-	ns
t_{AH}	Address Hold Time	15	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	10	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Clock Low Time	20	-	ns
t_{CLKH}	Clock High Time	20	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

(V_{DD}-V_{SS} = 2.4V to 2.6V, V_{DDIO} = 1.65V, V_{CI} = 3.3V, T_a = 25℃)

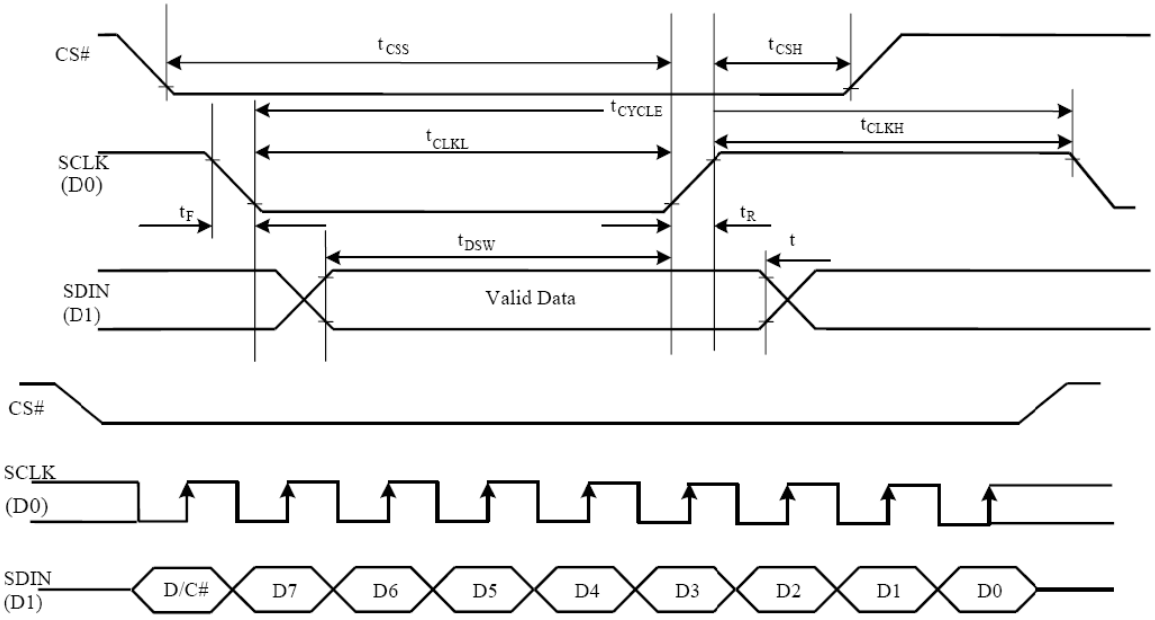




3.5.4 Serial Interface Timing Characteristics: (3-wire SPI)

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	10	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Clock Low Time	20	-	ns
t_{CLKH}	Clock High Time	20	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

(V_{DD}-V_{SS} = 2.4V to 2.6V, V_{DDIO} = 1.6V, V_{CI} = 3.3V, T_a = 25℃)



4 OPTICAL SPECIFICATION

4.1 OPTICAL CHARACTERISTICS

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness	L_{br}	Note 1	60	80	-	cd/m^2
C.I.E. (Yellow)	(x) (y)	C.I.E. 1931	0.46 0.45	0.50 0.49	0.54 0.53	
Dark Room Contrast	CR		-	>10,000:1	-	
Viewing Angle			-	Free	-	degree

Optical measurement taken at VCI = 2.8V, VCC = 15V.

Note 1:Brightness (L_{br}) and Supply Voltage for Display (VCC) are subject to the change of the panel characteristics and the customer's request.

5 FUNCTIONAL SPECIFICATION

5.1 COMMANDS

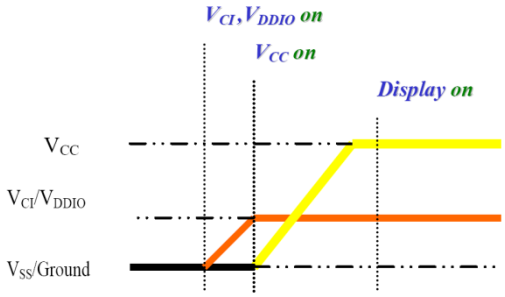
Refer to the Technical Manual for the SSD1322

5.2 POWER DOWN AND UP SEQUENCE

To protect the panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. Such that panel has enough time to charge and discharge before/after operation.

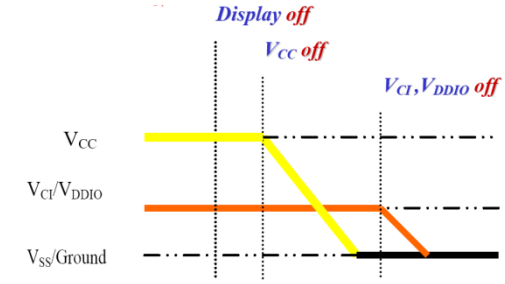
5.2.1 Power up Sequence:

1. Power up V_{CI} & V_{DDIO}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{CC}
6. Delay 200ms (when V_{CC} is stable)
7. Send Display on command



5.2.2 Power down Sequence:

1. Send Display off command
2. Power down V_{CC}
3. Delay 100ms (when V_{CC} is reach 0 and panel is completely discharges)
4. Power down V_{CI} & V_{DDIO}



Notes:

1) Since an ESD protection circuit is connected between VCI, VDDIO and VCC inside the driver IC, VCC becomes lower than VCI whenever VCI, VDDIO is ON and VCC is OFF.
2) VCC should be kept float (disable) when it is OFF.
3) Power Pins (VCI, VDDIO) can never be pulled to ground under any circumstance.
4) VCI, VDDIO should not be power down before VCC power down.

5.3 RESET CIRCUIT

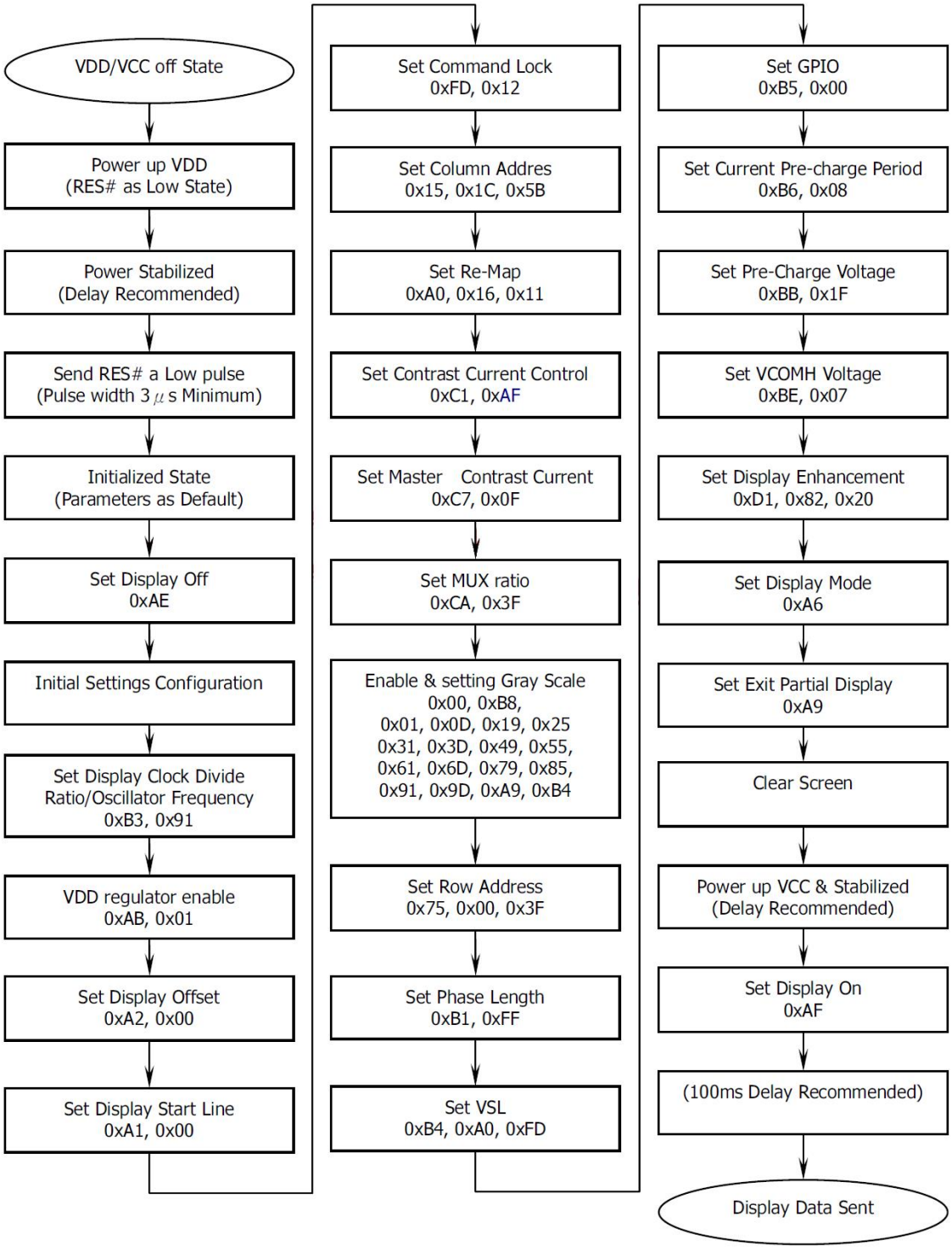
When RES# input is low, the chip initialized with the following status:

1. Display is OFF
2. 480x128 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4. Display start line is set at display RAM address 0
5. Column address counter is set at 0
6. Normal scan direction of the COM outputs
7. Contrast control registers is set at 7Fh

5.4 ACTUAL APPLICATION EXAMPLE

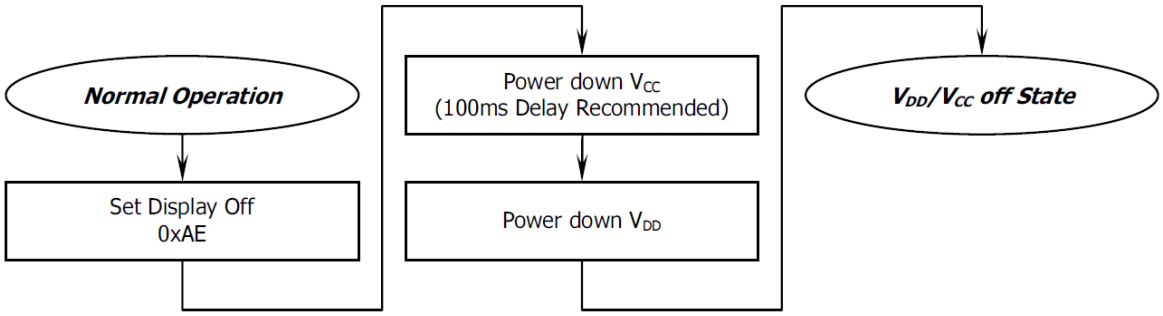
Command usage and explanation of an actual example

<Power up Sequence>

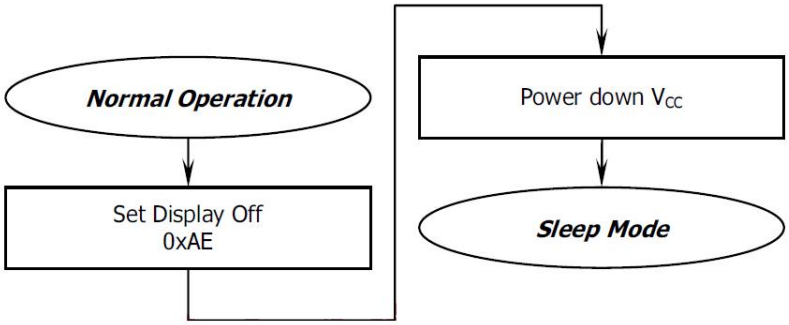


If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

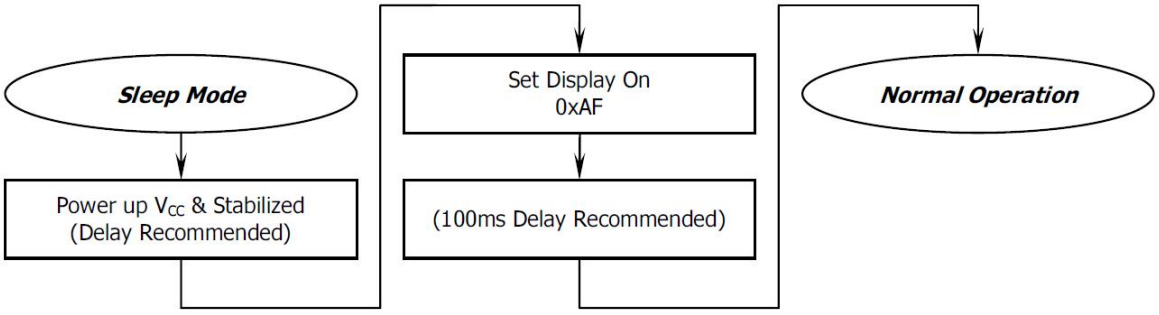
<Power down Sequence>



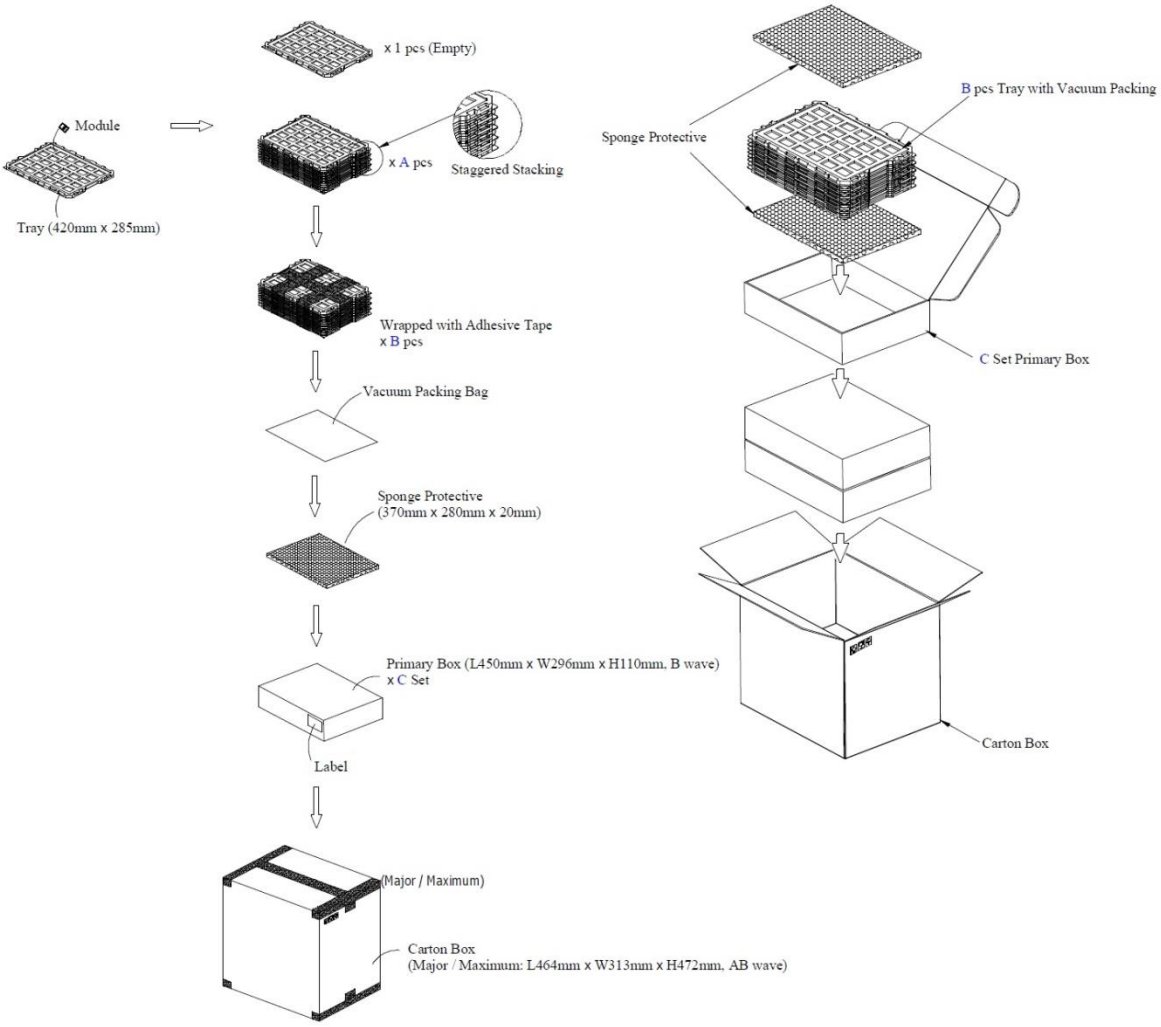
<Entering Sleep Mode>



<Exiting Sleep Mode>



6 PACKAGING



12 pieces per tray
21 trays per box (Including 1 empty tray)
1~4 boxes per carton

6.1 LABELLING AND MARKING

DENSITRON
DD-12864YW-13A
TW YYMM

7 QUALITY ASSURANCE SPECIFICATION

7.1 CONFORMITY

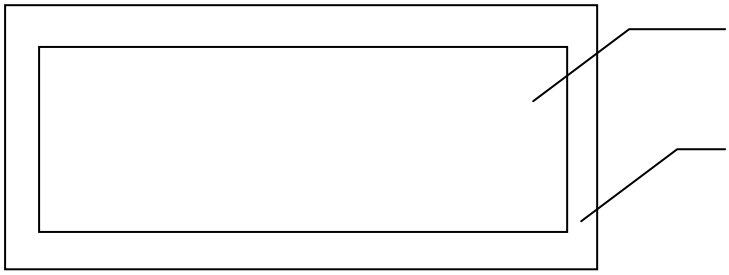
The performance, function and reliability of the shipped products conform to the Product Specification.

7.2 DELIVERY ASSURANCE

7.2.1 Delivery inspection standards

- IPC-AA610 rev. C, class 2 electronic assemblies standard

7.2.2 Zone definition

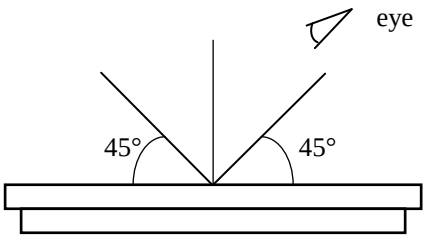


7.2.3 Visual inspection

Test and measurement to be conducted under following conditions：

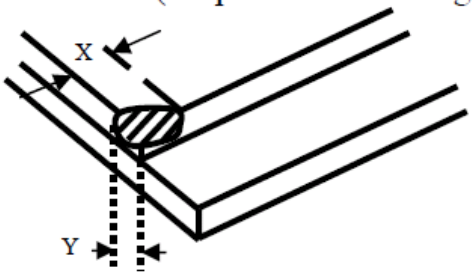
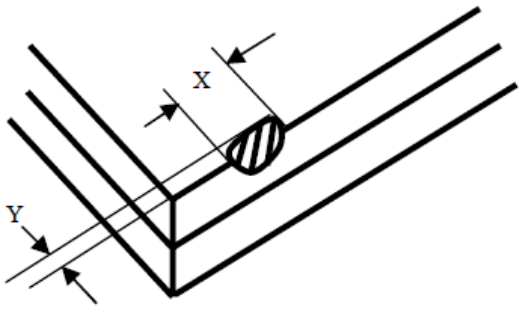
Temperature:	23±5℃
Humidity:	55±15%RH
Fluorescent lamp:	30 W
Distance between the Panel & Eyes of the Inspector:	≧30cm
Distance between the Panel & the lamp:	≧50cm

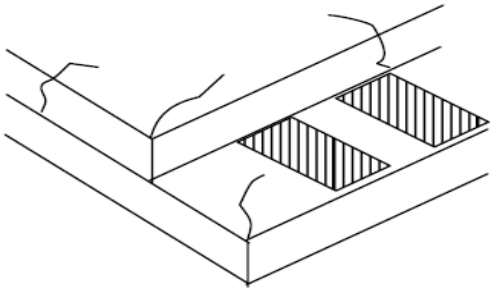
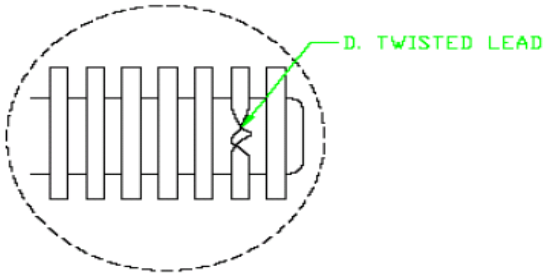
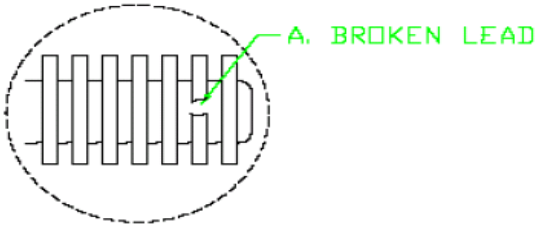
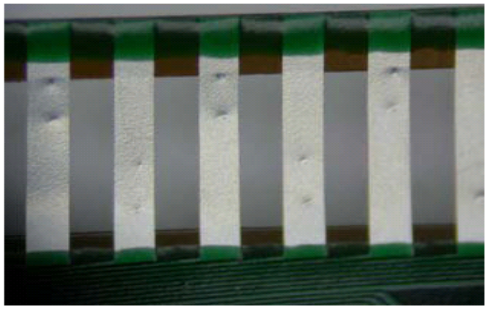
Finger glove (or finger cover) must be worn by the inspector.
Inspection table or jig must be anti-electrostatic

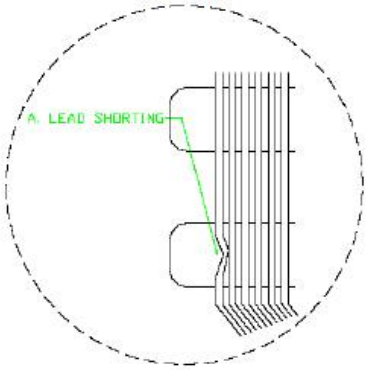
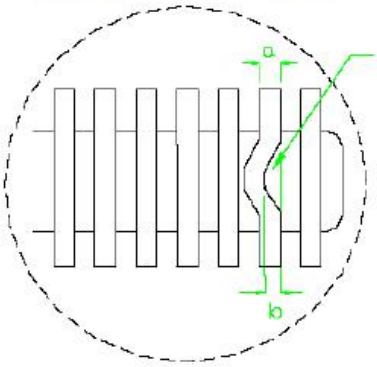
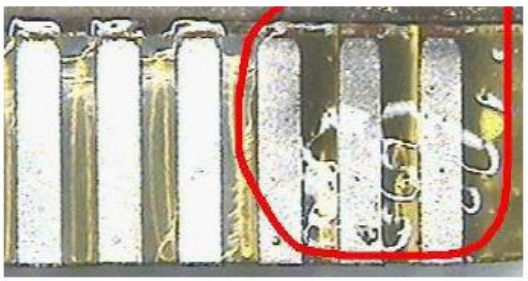


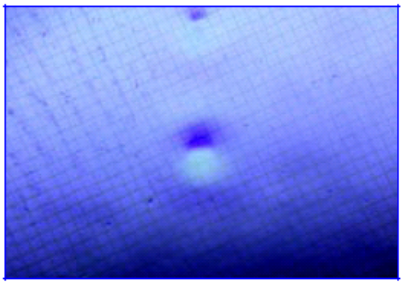
7.2.4 Standard of appearance inspection

Partition	AQL	Definition
Major	0.65	Defects in Pattern Check (Display On)
Minor	1.0	Defects in Cosmetic Check (Display Off)

Check Item	Classification	Criteria
Panel General Chipping	Minor	X > 6 mm (Along with Edge) Y > 1 mm (Perpendicular to edge)  

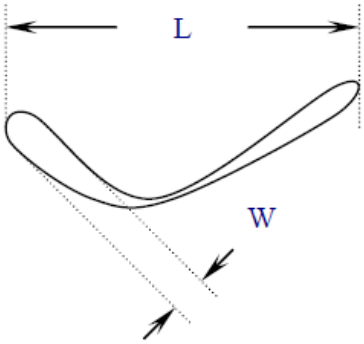
Check Item	Classification	Criteria
Panel Crack	Minor	Any crack is not allowable. 
Cupper Exposed (Even Pin or Film)	Minor	Not Allowable by Naked Eye Inspection
Film or Trace Damage	Minor	
Terminal Lead Twist	Minor	Not Allowable 
Terminal Lead Broken	Minor	Not Allowable 
Terminal Lead Prober Mark	Acceptable	

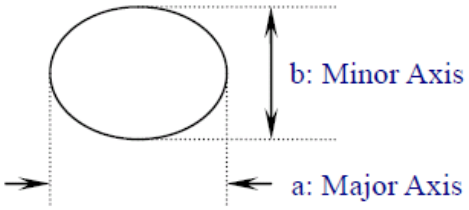
Check Item	Classification	Criteria
Terminal Lead Bent (Not Twist or Broken)	Minor	NG if any bent lead cause lead shorting. 
	Minor	NG for horizontally bent lead more than 50% of its width. 
Glue or Contamination on Pin (Couldn't Be Removed by Alcohol)	Minor	
Ink Marking on Back Side of panel (Exclude on Film)	Acceptable	Ignore for Any

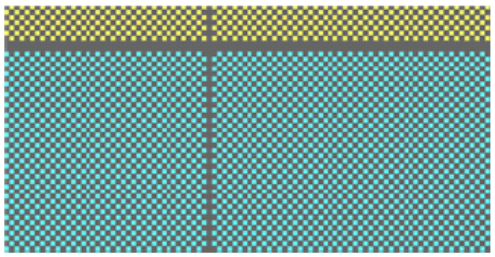
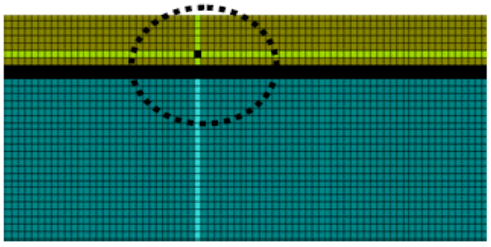
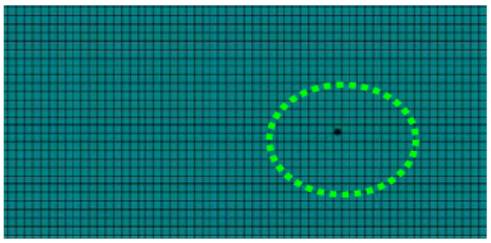
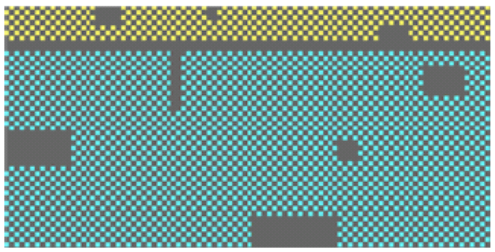
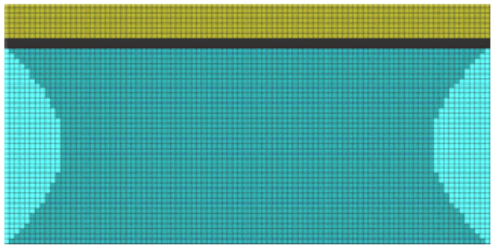
Check Item	Classification	Criteria
Any Dirt & Scratch on Polarizer's Protective Film	Acceptable	Ignore for not Affect the Polarizer
Scratches, Fiber, Line-Shape Defect (On Polarizer)	Minor	$W \le 0.1$ Ignore $W > 0.1, L \le 2$ $n \le 1$ $L > 2$ $n = 0$
Dirt, Black Spot, Foreign Material, (On Polarizer)	Minor	$\Phi \le 0.1$ Ignore $0.1 < \Phi \le 0.25$ $n \le 1$ $0.25 < \Phi$ $n = 0$
Dent, Bubbles, White spot (Any Transparent Spot on Polarizer)	Minor	$\Phi \le 0.5$ ➔ Ignore if no Influence on Display $0.5 < \Phi$ $n = 0$ 
Fingerprint, Flow Mark (On Polarizer)	Minor	Not Allowable

* Protective film should not be tear off when cosmetic check.

** Definition of W & L & Φ (Unit: mm): $\Phi = (a + b) / 2$





Check Item	Classification	Criteria
No Display	Major	
Flicker	Major	Not Allowable
Missing Line	Major	
Pixel Short	Major	
Darker Pixel	Major	
Wrong Display	Major	
Un-uniform	Major	

7.3 DEALING WITH CUSTOMER COMPLAINTS

7.3.1 Non-conforming analysis

Purchaser should supply Densitron with detailed data of non-conforming sample.
After accepting it, Densitron should complete the analysis in two weeks from receiving the sample.
If the analysis cannot be completed on time, Densitron must inform the purchaser.

7.3.2 Handling of non-conforming displays

If any non-conforming displays are found during customer acceptance inspection which Densitron is clearly responsible for, return them to Densitron.
Both Densitron and customer should analyse the reason and discuss the handling of non-conforming displays when the reason is not clear.
Equally, both sides should discuss and come to agreement for issues pertaining to modification of Densitron quality assurance standard.

8 RELIABILITY SPECIFICATION

8.1 RELIABILITY TESTS

Test Item	Test Condition	Evaluation and assessment
High Temperature Operation	70°C, 240 hrs	The brightness should be greater than 50% of the initial brightness. The operational functions work.
Low Temperature Operation	-40°C, 240 hrs	
High Temperature Storage	85°C, 240 hrs	
Low Temperature Storage	-40°C, 240 hrs	
High Temperature & High Humidity Storage	60°C, 90% RH, 120 hrs	
Thermal Shock Storage	-40°C ↔85°C, 24 cycles 60 min. dwell	

- The samples used for above tests do not include polarizer.
- No moisture condensation is observed during tests.

8.1.1 FAILURE CHECK STANDARD

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure teat at 23±5 ℃ ; 55±15% RH

8.2 LIFE TIME

Item	Description
1	Function, performance, appearance, etc. shall be free from remarkable deterioration within 10,000 hours under ordinary operating and storage conditions of room temperature (25±10 °C), normal humidity (45±20% RH), and in area not exposed to direct sunlight.
2	End of lifetime is specified as 50% of initial brightness.

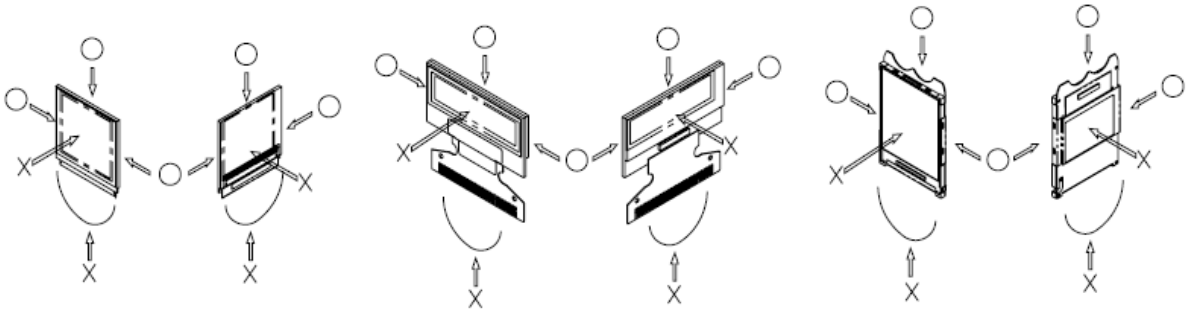
8.3 FAILURE CHECK STANDARD

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5°C; 55±15% RH.

9 HANDLING PRECAUTIONS

9.1 HANDLING PRECAUTIONS

1) Since the display panel is being made of glass, do not apply mechanical impacts such us dropping from a high position.
2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.
3) If pressure is applied to the display surface or its neighborhood of the OEL display module, the cell structure may be damaged and be careful not to apply pressure to these sections.
4) The polarizer covering the surface of the OEL display module is soft and easily scratched. Please be careful when handling the OEL display module.
5) When the surface of the polarizer of the OEL display module has soil, clean the surface. It takes advantage of by using following adhesion tape.
   * Scotch Mending Tape No. 810 or an equivalent
   Never try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy.
   Also, pay attention that the following liquid and solvent may spoil the polarizer:
   * Water
   * Ketone
   * Aromatic Solvents
6) Hold OEL display module very carefully when placing OEL display module into the system housing. Do not apply excessive stress or pressure to OEL display module. And, do not over bend the film with electrode pattern layouts. These stresses will influence the display performance. Also, secure sufficient rigidity for the outer cases.



7) Do not apply stress to the LSI chips and the surrounding molded sections.
8) Do not disassemble nor modify the OEL display module.
9) Do not apply input signals while the logic power is off.
10) Pay sufficient attention to the working environments when handing OEL display modules to prevent occurrence of element breakage accidents by static electricity.
    * Be sure to make human body grounding when handling OEL display modules.
    * Be sure to ground tools to use or assembly such as soldering irons.
    * To suppress generation of static electricity, avoid carrying out assembly work under dry environments.

* Protective film is being applied to the surface of the display panel of the OEL display module. Be careful since static electricity may be generated when exfoliating the protective film.

11) Protection film is being applied to the surface of the display panel and removes the protection film before assembling it. At this time, if the OEL display module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).
12) If electric current is applied when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

9.2 STORAGE PRECAUTIONS

1) When storing OEL display modules, put them in static electricity preventive bags avoiding exposure to direct sun light nor to lights of fluorescent lamps, etc. and, also, avoiding high temperature and high humidity environments or low temperature (less than 0°C) environments. (We recommend you to store these modules in the packaged state when they were shipped from Densitron Technologies Plc.) At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.
2) If electric current is applied when water drops are adhering to the surface of the OEL display module, when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

9.3 DESIGNING PRECAUTIONS

1) The absolute maximum ratings are the ratings which cannot be exceeded for OEL display module, and if these values are exceeded, panel damage may be happen.
2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the VIL and VIH specifications and, at the same time, to make the signal line cable as short as possible.
3) We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (VDD). (Recommend value: 0.5A)
4) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighboring devices.
5) As for EMI, take necessary measures on the equipment side basically.
6) When fastening the OEL display module, fasten the external plastic housing section.
7) If power supply to the OEL display module is forcibly shut down by such errors as taking out the main battery while the OEL display panel is in operation, we cannot guarantee the quality of this OEL display module.
8) The electric potential to be connected to the rear face of the IC chip should be as follows: US2066
   * Connection (contact) to any other potential than the above may lead to rupture of the IC.

9.4 OTHER PRECAUTIONS

1) When an OEL display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur. Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored. Also, there will be no problem in the reliability of the module.
2) To protect OEL display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the OEL display modules.
   * Pins and electrodes
   * Pattern layouts such as the FPC
3) With this OEL display module, the OEL driver is being exposed. Generally speaking, semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if this OEL driver is exposed to light, malfunctioning may occur.
   * Design the product and installation method so that the OEL driver may be shielded from light in actual usage.
   * Design the product and installation method so that the OEL driver may be shielded from light during the inspection processes.
4) Although this OEL display module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed. It therefore is necessary to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.
5) We recommend you to construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.

9.5 PRECAUTIONS WHEN DISPOSING OF THE OEL DISPLAY MODULES

1) Request the qualified companies to handle industrial wastes when disposing of the OEL display modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.

10 SUPPORTED ACCESSORIES

10.1 DUO KIT

Densitron has developed an easy to use yet powerful development and demonstration tool for driving its range of Passive Matrix OLED displays from the USB port of a PC.
DUO (Densitron USB OLED) kit is hot pluggable and does not require extra cables or power supply to run, allowing users to be up and running in minutes.

The kit consists of an OLED display with transition Board, USB controller card, mini USB cable and a CD with software application and drivers.

Part number: UNDER DEVELOPMENT

10.2 TRANSITION BOARD CARD

A Transition board card is like a daughterboard which is meant to be a circuit board for connections between the baseboards (DUO).
It has connector pins for interfacing between the display and the baseboards.
It also includes the OLED display.
Part number: UNDER DEVELOPMENT

10.3 CONNECTOR BOARD CARD

A Connector board card is also a daughterboard which is a circuit board for connection between a microprocessor or microcontroller (customer's system).
Part number: UNDER DEVELOPMENT

10.4 CONNECTOR

Type: ZIF connector

No. of connections	Pitch (mm)	Manufacturer	Manufacturer part no.	Distributor part no.
30	0.50	Omron	XF2M-3015-1A	Farnell/1112560 Digikey/ OR723CT-ND