OLED DISPLAY MODULE

Product Specification

CUSTOMER	**Standard**	
PRODUCT NUMBER	**DD-2C16BE-1A**	
CUSTOMER APPROVAL		

INTERNAL APPROVALS		
Product Mgr	Doc. Control	Electr. Eng
Richard Applin	**Richard Applin**	**Alan Wang**
Date: 16 July 13	Date: 16 July 13	Date: 16 July 13

TABLE OF CONTENTS

REVISION RECORD

Rev.	Date	Page	Chapt.	Comment	ECR no.
A	16 July13			First Issue	

1 MAIN FEATURES

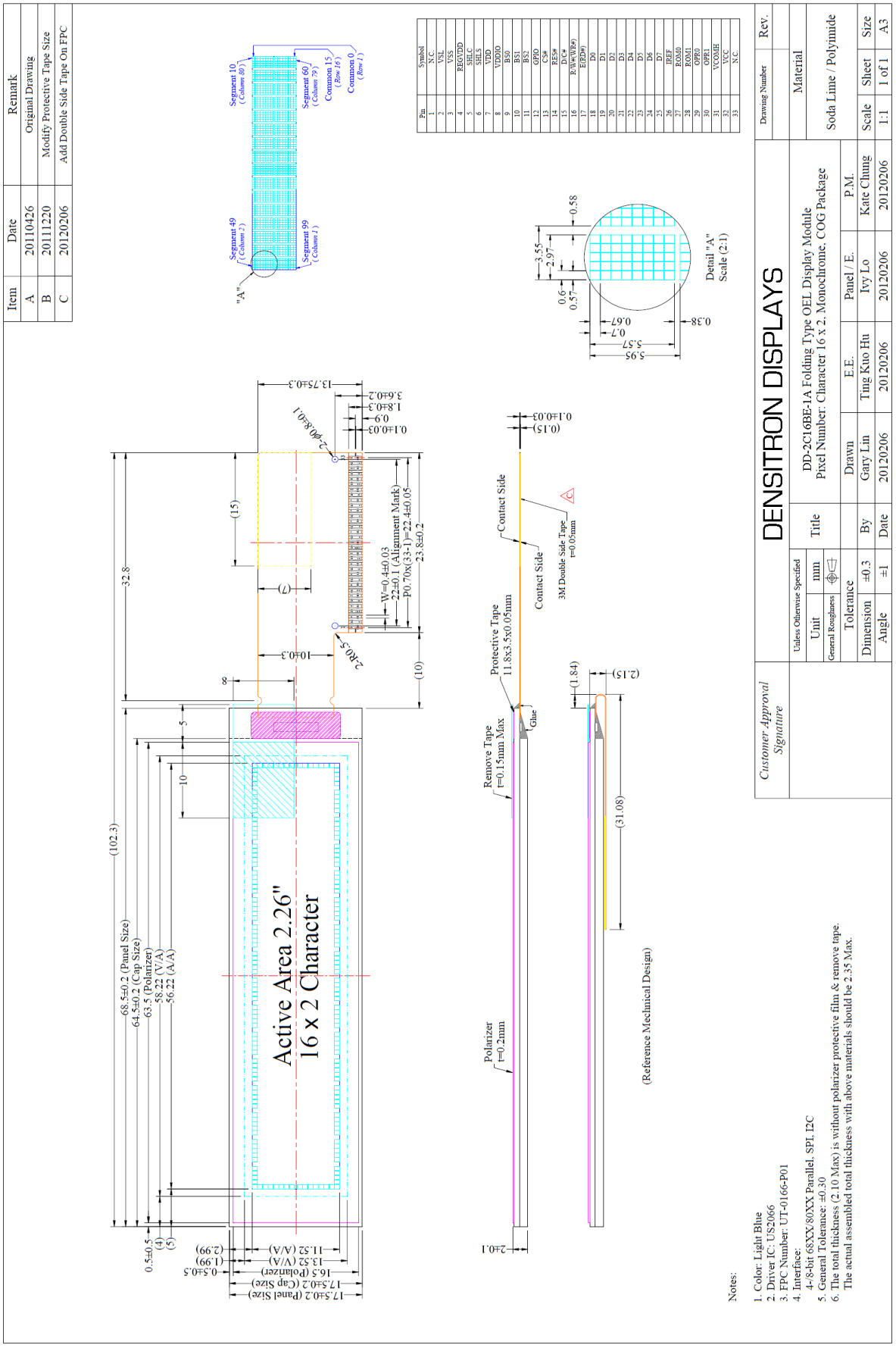
ITEM	CONTENTS
Characters x lines	16 x 2
Character Font	5 x 8
Overall Dimensions	68.50 x 17.50 x 2.00 mm
Colour	Light Blue
Active Area	56.22 x 11.52 mm
Viewing Area	58.22 x 13.52 mm
Display Mode	Passive Matrix (2.26”)
Driving Method	1/16 duty
Driver IC	US2066
Operating temperature	-40 ~ +85 ºC
Storage temperature	-40 ~ +90 ºC

2 MECHANICAL SPECIFICATION

2.1 MECHANICAL CHARACTERISTICS

ITEM	CHARACTERISTIC	UNIT
Characters x lines	16 x 2	
Overall Dimensions	68.50 x 17.50 x 2.00	mm
Viewing Area	58.22 x 13.52	mm
Active Area	56.22 x 11.52	mm
Dot Size	0.57 x 0.67	mm
Dot Pitch	0.60 x 0.70	mm
Character size	2.97 x 5.57	mm
Weight	4.98	g
IC Controller/Driver	US2066	

2.2 MECHANICAL DRAWING



3 ELECTRICAL SPECIFICATION

3.1 ABSOLUTE MAXIMUM RATINGS

VSS = 0 V, Ta = 25 °C

Item	Symbol	Min	Max	Unit	Note
Supply Voltage for logic	V_{DD}	-0.3	6	V	Note 1, 2
Supply voltage for I/O Pins	V_{DDIO}	-0.3	6	V	
Supply voltage for Display	V_{CC}	0	15	V	
Operating Temperature	Top	-40	85	°C	Note 3
Storage Temperature	Tst	-40	90	°C	

Note 1: All the above voltages are on the basis of "VSS=0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent damage to the module may occur. Also for normal operations it's desirable to use this module under the conditions according to Section 3.2 "Electrical Characteristics". If this module is used beyond these conditions the module may malfunction and the reliability could deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80°C.

3.2 ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Logic	V_{DD}	Low Voltage Mode	2.4	2.8	VDDIO	V
		5V Voltage Mode	-	-	-	V
Supply Voltage for I/O	V_{DDIO}	Low Voltage Mode	2.4	2.8	3.6	V
		5V Voltage Mode	4.4	5.0	5.5	V
Supply Voltage for Display	V_{CC}	Note 1	8.5	9.0	9.5	V
High Level Input	V_{IH}	IOUT=0.1mA, 3.3MHz	0.8xV_{DDIO}	-	V_{DDIO}	V
Low Level Input	V_{IL}		0	-	0.2 x VDDIO	V
High Level Output	V_{OH}		0.9 x VDDIO	-	VDDIO	V
Low Level Output	V_{OL}		0	-	0.1 x VDDIO	V
Operating current for VDD	IDD	-	-	180	300	µA
Operating current for VCC	ICC	Note 2	-	5.4	6.8	mA
		Note 3	-	8.0	10.0	
		Note 4	-	13.6	17.0	
Sleep mode current for VDD	IDD SLEEP		-	1	10	µA
Sleep mode current for VCC	ICC SLEEP		-	2	10	µA

Note 1: Brightness (Lbr) and Supply Voltage for Display (VCC), are subject to the change of the panel characteristics

Note 2: V_{DDIO} = 2.8V or 5.0V, V_{CC} = 9.0V, 30% display area turned on.

Note 3: V_{DDIO} = 2.8V or 5.0V, V_{CC} = 9.0V, 50% display area turned on.

Note 4: V_{DDIO} = 2.8V or 5.0V, V_{CC} = 9.0V, 100% display area turned on.

3.3 INTERFACE PIN ASSIGNMENT

<table>
<tr><th>No.</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>1</td><td>N.C.(GND)</td><td>-</td><td>Reserved Pin (Supporting Pin)
The supporting pin can reduce the influence from stress on the function pins. This pin must be connected to external ground</td></tr>
<tr><td>2</td><td>VSL</td><td>P</td><td>Segment Voltage Reference Pin
When external VSL is not used, this pin should be left open.
When external VSL is used, connect with resistor and diode to ground.</td></tr>
<tr><td>3</td><td>VSS</td><td>P</td><td>Ground of Logic Circuit
This is a ground pin. It also acts as a reference for the logic pins, the OEL driving voltages and the analogue circuits. It must be connected to external ground.</td></tr>
<tr><td>4</td><td>REGVDD</td><td>I</td><td>Internal VDD Regulator Selection Pin
When this pin is pulled HIGH, internal VDD regulator is enabled (VDD outputs 3.3V).
When this pin is pulled LOW, internal VDD regulator is disabled (VDD outputs 5V).</td></tr>
<tr><td>5</td><td>SHLC</td><td>I</td><td>COM Scan Direction Selection
This pin is used to determine the Common output scanning direction
<table>
<tr><td>SHLC</td><td>COM scan direction</td></tr>
<tr><td>0</td><td>COM0 to COM31</td></tr>
<tr><td>1</td><td>COM31 to COM0</td></tr>
</table></td></tr>
<tr><td>6</td><td>SHLS</td><td>I</td><td>SEG Direction Selection
This pin is used to determine the SEG direction
<table>
<tr><td>SHLS</td><td>SEG direction</td></tr>
<tr><td>0</td><td>SEG99 to SEG0</td></tr>
<tr><td>1</td><td>SEG0 to SEG99</td></tr>
</table></td></tr>
<tr><td>7</td><td>VDD</td><td>P</td><td>Power Supply for Logic
This is a voltage supply pin. It can be supplied externally or regulated internally.
In 3V IO mode, this is a power input pin.
In 5V IO mode, the output is around 3.3V.
A capacitor should be connected between VDD and VSS under all circumstances</td></tr>
<tr><td>8</td><td>VDDIO</td><td>P</td><td>Power Supply for Interface Logic Level
It should match with the MCU interface voltage level and must be connected to external source</td></tr>
<tr><td>9</td><td>BS0</td><td rowspan="2">I</td><td rowspan="2">Communicating Protocol Select
These pins are MCU interface selection input. See the following table:
<table>
<tr><td></td><td>BS0</td><td>BS1</td><td>BS2</td></tr>
<tr><td>Serial Interface</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Invalid</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>I2C</td><td>0</td><td>1</td><td>0</td></tr>
</table></td></tr>
<tr><td>10</td><td>BS1</td></tr>
</table>

<table>
<tr><td>11</td><td>BS2</td><td></td><td>
<table>
<tr><td>Invalid</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>8 bit 68XX-parallel</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>4 bit 68XX-parallel</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>8 bit 80XX-parallel</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>4 bit 80XX-parallel</td><td>1</td><td>1</td><td>1</td></tr>
</table>
</td></tr>
<tr><td>12</td><td>GPIO</td><td>I/O</td><td>It is a reserved pin and is recommended to keep it floating.</td></tr>
<tr><td>13</td><td>CS#</td><td>I</td><td>Chip Select
This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.</td></tr>
<tr><td>14</td><td>RES#</td><td>I</td><td>Power Reset for Controller and Driver
This pin is reset signal input. When the pin is low, initialization of the chip is executed.</td></tr>
<tr><td>15</td><td>D/C#</td><td>I</td><td>Data/Command Control
This is Data/Command control pin. When the pin is pulled high, the input at D7~D0 is treated as display data.
When the pin is pulled low, the input at D7~D0 will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.

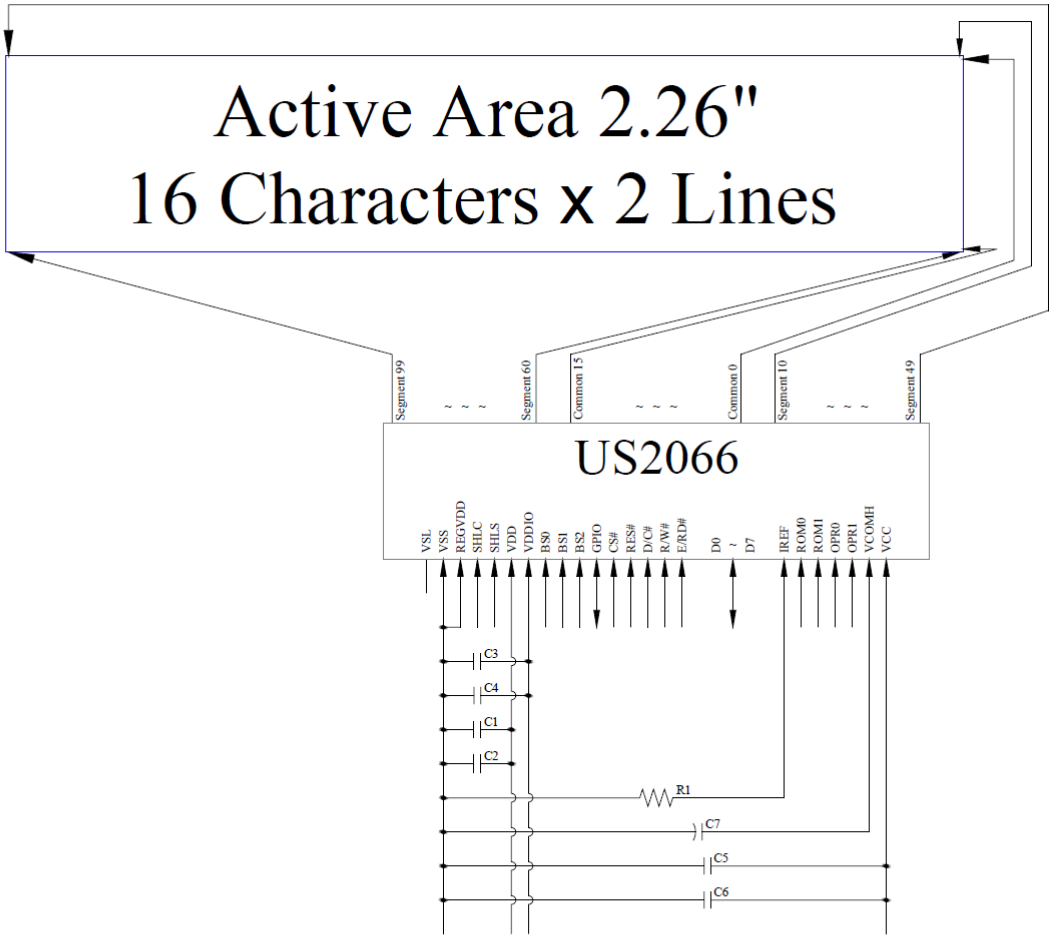
When the pin is pulled high and serial interface mode is selected, the data at SDIN is treated as data. When it is pulled low the data at SDIN will be transferred to the command register. In I2C mode, this pin acts as SA0 for slave address selection.</td></tr>
<tr><td>16</td><td>R/W#</td><td>I</td><td>Read/Write Select or Write
This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to “High” for read mode and pull it to “Low” for write mode.

When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin and the CS# are pulled low.</td></tr>
<tr><td>17</td><td>E/RD#</td><td>I</td><td>Read/Write Enable or Read
This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low.

When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low.</td></tr>
<tr><td>18~25</td><td>D0~D7</td><td>I/O</td><td>Host Data Input/Output Bus
These pins are 8-bit bi-directional data bus to be connected to the microprocessor’s data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK. When I2C mode is selected, D2, D1 should be tied together and serve as SDAout, SDAin in application and D0 is the serial clock input SCL</td></tr>
</table>

<table>
<tr><td>26</td><td>IREF</td><td>I</td><td>Current Reference for Brightness Adjustment
This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current at 12.5uA.</td></tr>
<tr><td>27</td><td>ROM0</td><td rowspan="2">I</td><td rowspan="2">Character ROM Selection
These pins are used to select Character ROM. See the following table:
<table>
<tr><th>ROM</th><th>ROM0</th><th>ROM1</th></tr>
<tr><td>A</td><td>0</td><td>0</td></tr>
<tr><td>B</td><td>1</td><td>0</td></tr>
<tr><td>C</td><td>0</td><td>1</td></tr>
<tr><td>S/W selectable</td><td>1</td><td>1</td></tr>
</table></td></tr>
<tr><td>28</td><td>ROM1</td></tr>
<tr><td>29</td><td>OPR0</td><td rowspan="2">I</td><td rowspan="2">Select the number of Character Generator
These pins are used to select Character number of character generator. See the following table:
<table>
<tr><th>CGROM</th><th>CGRAM</th><th>OPR0</th><th>OPR1</th></tr>
<tr><td>256</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>248</td><td>8</td><td>1</td><td>0</td></tr>
<tr><td>250</td><td>6</td><td>0</td><td>1</td></tr>
<tr><td>240</td><td>8</td><td>0</td><td>0</td></tr>
</table></td></tr>
<tr><td>30</td><td>OPR1</td></tr>
<tr><td>31</td><td>VCOMH</td><td>O</td><td>Voltage Output High Level for COM Signal
This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and VSS.</td></tr>
<tr><td>32</td><td>VCC</td><td>P</td><td>Power Supply for OEL Panel
This is the most positive voltage supply pin of the chip. A stabilization capacitor should be connected between this pin and VSS when the converter is used. It must be supplied externally.</td></tr>
<tr><td>33</td><td>N.C.</td><td>-</td><td>Reserved Pin (Supporting Pin)
The supporting pin can reduce the influence from stress on the function pins. This pin must be connected to external ground</td></tr>
</table>

3.4 BLOCK DIAGRAM



MCU Interface Selection: BS0, BS1 and BS2
Pins connected to MCU interface: CS#, RES#, D/C#, R/W#, E/RD#, and D0~D7
* SHLC, SHLC, ROM0, ROM1, OPR0 and OPR1 should be configured.

C1, C3, C5: 0.1μF
C2, C4: 4.7μF
C6: 10μF
C7: 4.7μF / 25V Tantalum Capacitor
R1: 300kΩ, R1 = (Voltage at IREF - VSS) / IREF

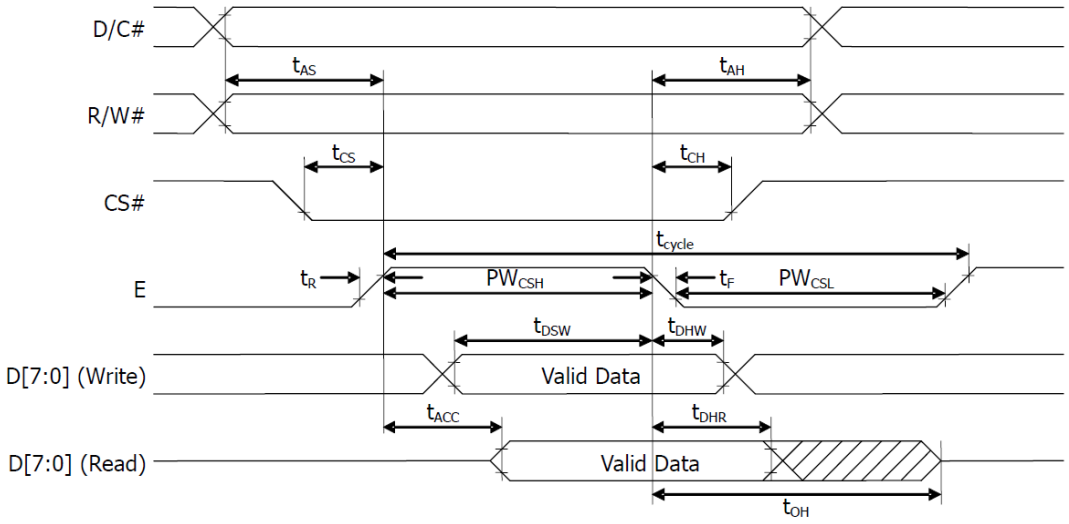
3.5 TIMING CHARACTERISTICS

3.5.1 AC CHARACTERISTICS

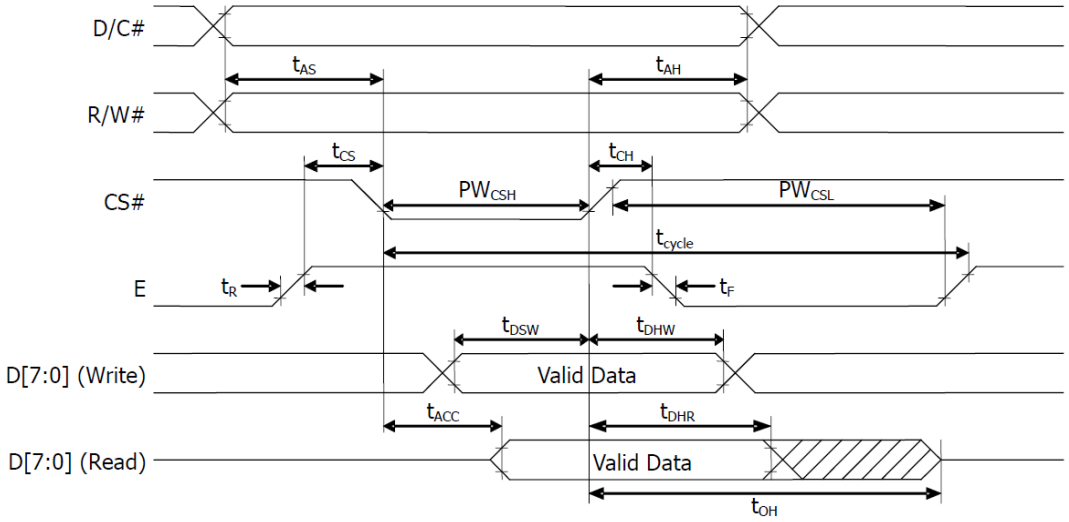
3.5.1.1 68XX-Series MPU Parallel Interface Timing Characteristics

VDDIO-VSS = 2.4V to 3.6V / 4.4V to 5.5V, Ta = 25˚C

Symbol	Description	Min	Max	Unit
tcycle	System Cycle Time	400	-	ns
t_{AS}	Address Setup Time	13	-	ns
t_{AH}	Address Hold Time	17	-	ns
t_{DSW}	Write Data Setup Time	35	-	ns
t_{DHW}	Write Data Hold Time	18	-	ns
t_{DHR}	Read Data Hold Time	13	-	ns
t_{OH}	Output Disable Time	10	90	ns
t_{ACC}	Access Time	-	125	ns
t_{CS}	Chip Select Time	0	-	ns
t_{CH}	Chip Select Hold Time	0	-	ns
PW_{CSL}	Chip Select Low Pulse Width (Read RAM)	250	-	ns
	Chip Select Low Pulse Width (Read Command)	250		
	Chip Select Low Pulse width (Write)	50		
PW_{CSH}	Chip Select High Pulse Width (Read)	155	-	ns
	Chip Select High Pulse Width (Write)	55		
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns



(CS# "Low Pulse Width" > E "High Pulse Width")

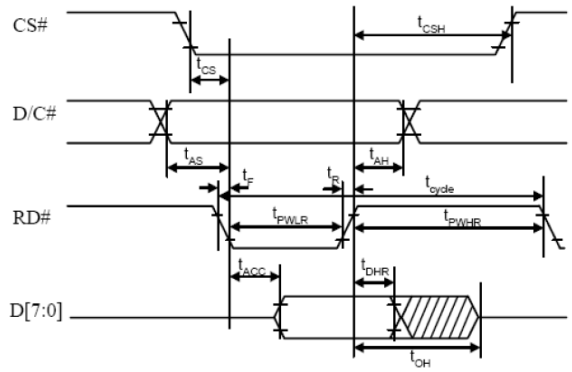


(CS# "Low Pulse Width" < E "High Pulse Width")

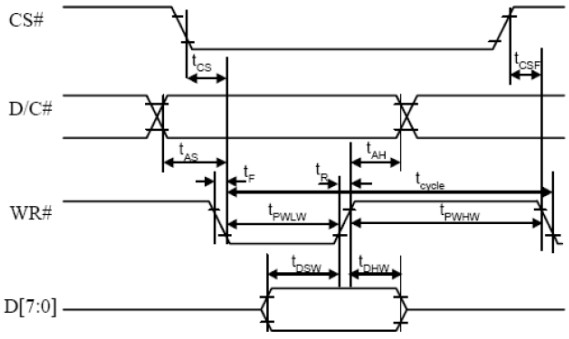
3.5.1.2 8080-Series MPU Parallel Interface Timing Characteristics

VDDIO-VSS = 2.4V to 3.6V / 4.4V to 5.5V, Ta = 25˚C

Symbol	Description	Min	Max	Unit
tcycle	Clock Cycle Time	400	-	ns
t_{AS}	Address Setup Time	13	-	ns
t_{AH}	Address Hold Time	17	-	ns
t_{DSW}	Write Data Setup Time	35	-	ns
t_{DHW}	Write Data Hold Time	18	-	ns
t_{DHR}	Read Data Hold Time	13	-	ns
t_{OH}	Output Disable Time	10	70	ns
t_{ACC}	Access Time	-	125	ns
t_{PWLR}	Read Low Time	250	-	ns
t_{PWLW}	Write Low Time	50	-	ns
t_{PWHR}	Read High Time	155	-	ns
t_{PWHW}	Write High Time	55	-	ns
t_{CS}	Chip Select Setup Time	0	-	ns
t_{CSH}	Chip Select Hold Time to Read Signal	0	-	ns
t_{CSF}	Chip Select Hold Time	0	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns



(*Read Timing*)

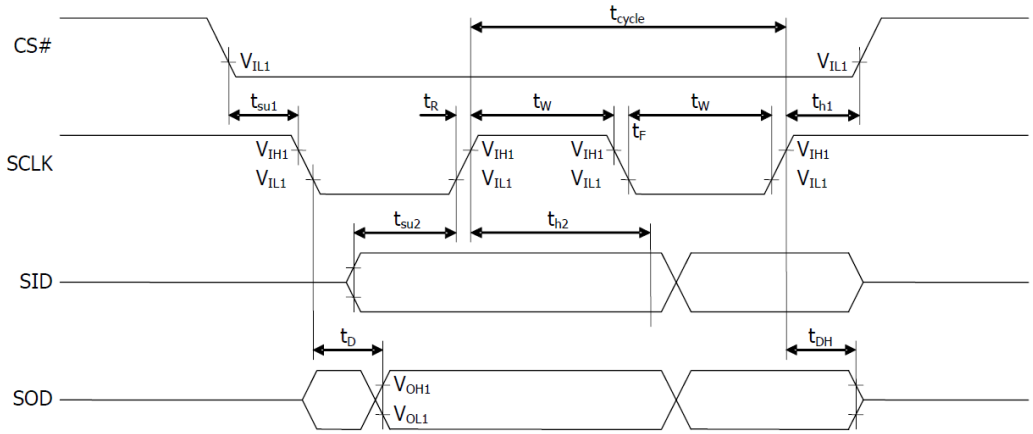


(*Write Timing*)

3.5.1.3 Serial Interface Timing Characteristics

VDDIO-VSS = 2.4V to 3.6V / 4.4V to 5.5V, Ta = 25˚C

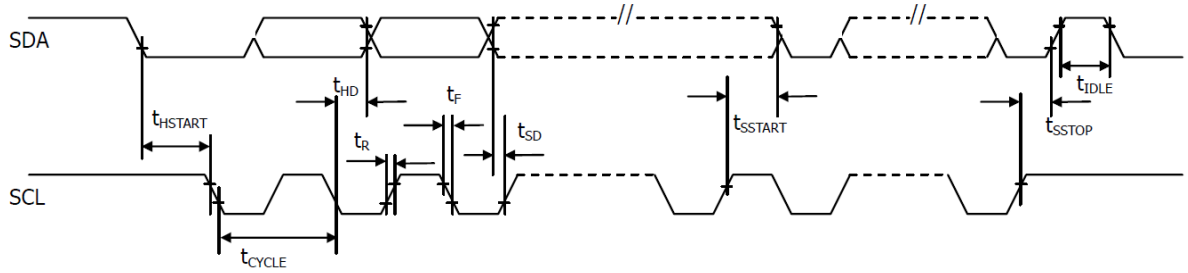
Symbol	Description	Min	Max	Unit
tcycle	Serial Clock Cycle Time	1	20	ns
t_{SU1}	Address Setup Time	60	-	ns
t_{H1}	Address Hold Time	20	-	ns
t_{SU2}	Chip Select Setup Time	200	-	ns
t_{H2}	Chip Select Hold Time	TBD	-	ns
t_D	Write Data Setup Time	-	TBD	ns
t_{DH}	Write Data Hold Time	10	-	ns
t_W	Serial Clock Low Time	400	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns



3.5.1.4 I²C Interface Timing Characteristics

VDDIO-VSS = 2.4V to 3.6V / 4.4V to 5.5V, Ta = 25˚C

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	us
t_{HSTART}	Start Condition Hold Time	0.6	-	us
t_{HD}	Data Hold Time (for "SDAOUT" Pin) Data	5	-	ns
	Hold Time (for "SDAIN" Pin)	300		
t_{SD}	Data Setup Time	100	-	ns
t_{SSTART}	Start Condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	us
t_{SSTOP}	Stop Condition Setup Time	0.6	-	us
t_R	Rise Time for Data and Clock Pin		300	ns
t_F	Fall Time for Data and Clock Pin		300	ns
t_{IDLE}	Idle Time before a New Transmission can Start	1.3	-	us



4 OPTICAL SPECIFICATION

4.1 OPTICAL CHARACTERISTICS

Characteristics	Symbol	Condition	Min	Typ	Max	Unit
Brightness	L_{br}	Note 5	60	80	-	cd/m^2
C.I.E.(Blue)	(X)	C.I.E. 1931	0.12	0.16	0.20	-
	(Y)		0.22	0.26	0.30	
Dark Room Contrast	CR		-	>10,000:1	-	-
Viewing Angle			-	Free	-	degree

* Optical measurement taken at V_{DDIO} = 2.8V or 5.0V, V_{CC} = 9.0V.

5 FUNCTIONAL SPECIFICATION

5.1 COMMANDS

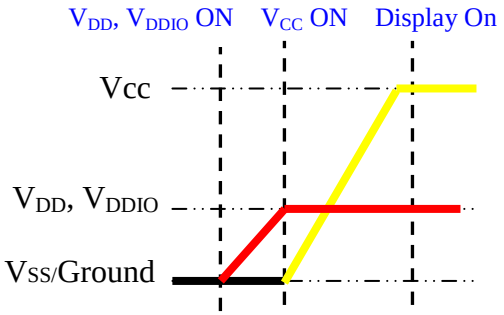
Please refer to the Technical Manual for the US2066

5.2 POWER UP/DOWN SEQUENCE

To protect panel and extend the panel lifetime, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the panel enough time to complete the action of charge and discharge before/after the operation.

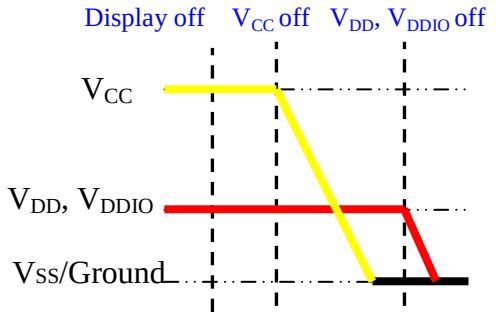
5.2.1 POWER UP SEQUENCE

1. Power up V_{DD} &V_{DDIO}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{CC}
6. Delay 100ms
(When Vcc is stable)
7. Send Display on command



5.2.2 POWER DOWN SEQUENCE

1. Send Display off command
2. Power down V_{CC}
3. Delay 100ms
(When V_{cc} reaches 0 and panel is Completely discharged)
4. Power down V_{DD} &V_{DDIO}



Conditions:

1) Since an ESD protection circuit is connected between VDD, VDDIO and VCC inside the driver IC, VCC becomes lower than VDD & VDDIO whenever VDD & VDDIO is ON and VCC is OFF.
2) VCC should be kept float (disable) when it is OFF.
3) Power Pins (VDD, VDDIO, and VCC) can never be pulled to ground under any circumstance.
4) VDD & VDDIO should not be power down before VCC power down.

5.3 RESET CIRCUIT

When RES# input is low, the chip is initialized with the following status:

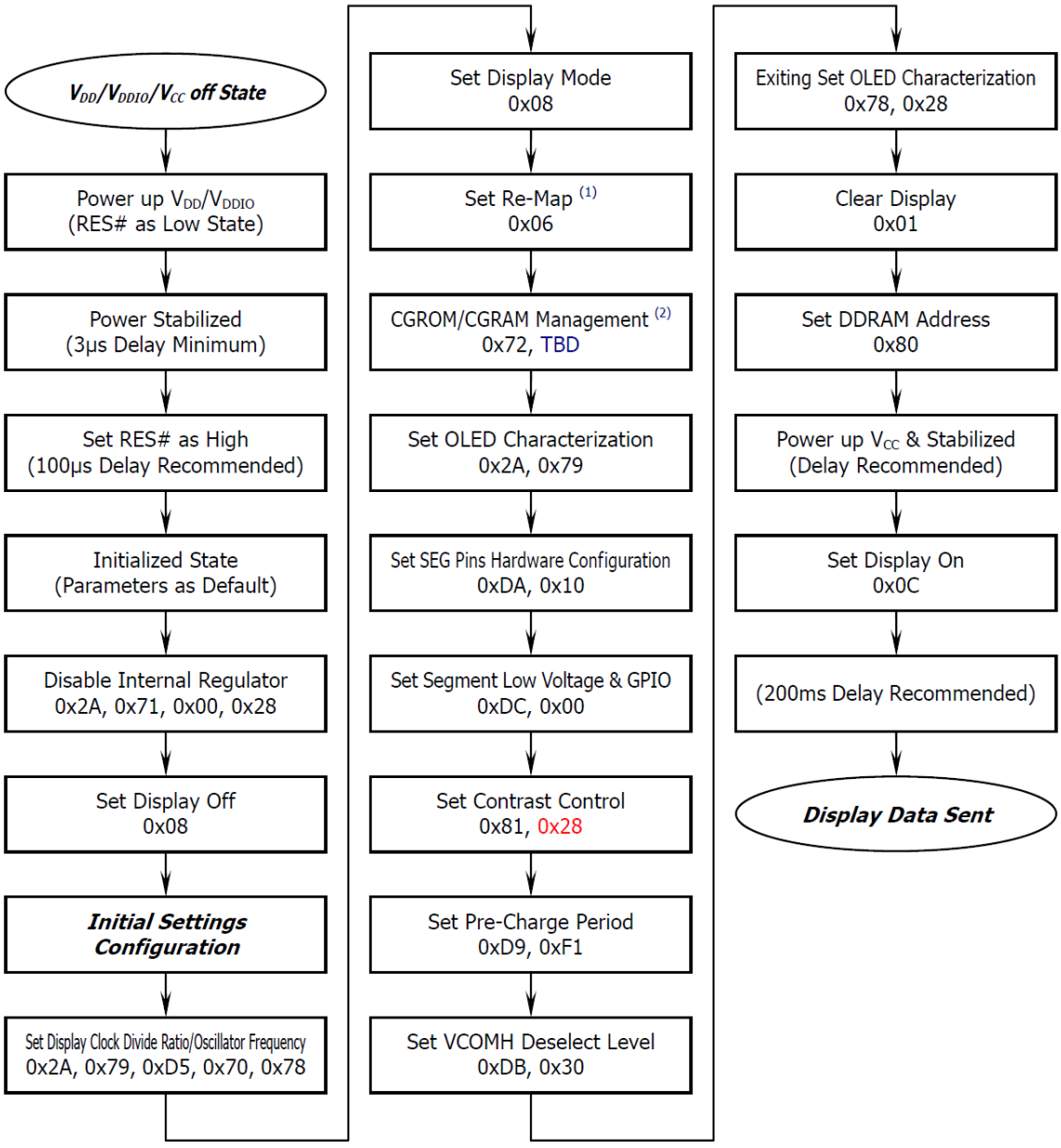
1. Display is OFF
2. 5×8 Character Mode
3. Display start position is set at display RAM address 0
4. CGRAM address counter is set at 0
5. Cursor is OFF
6. Blink is OFF
7. Contrast control register is set at 7Fh
8. OLED command set is disabled

5.4 ACTUAL APPLICATION EXAMPLE

Command usage and explanation of an actual example

5.4.1 Low Voltage I/O Application

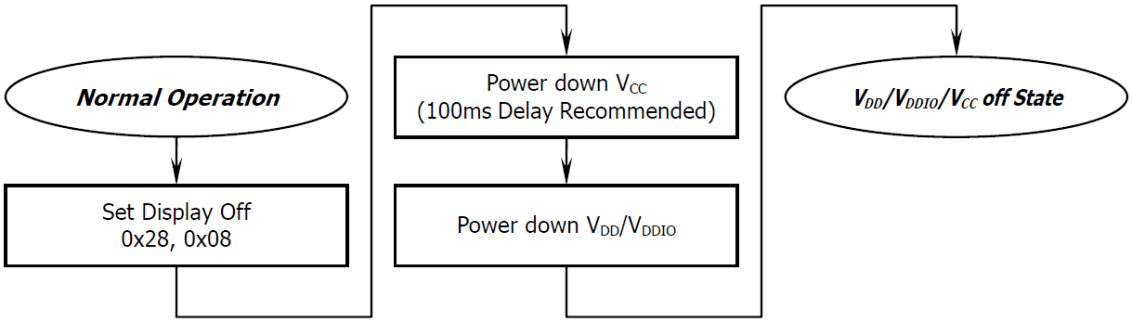
<Power up Sequence>



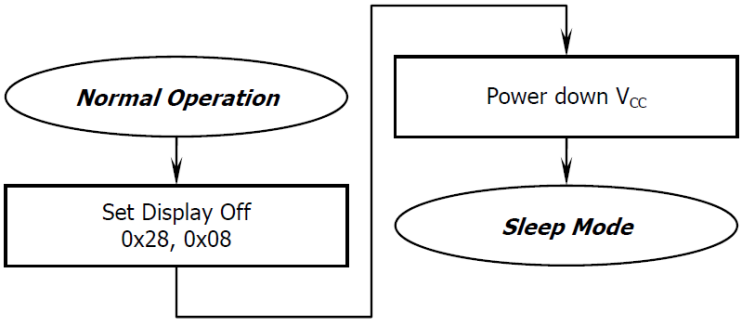
1) This command could be programmable or defined by pin configuration.
2) This command could be programmable or defined by pin configuration. The written value of the parameter should depend on the selection from Section 5.5

If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

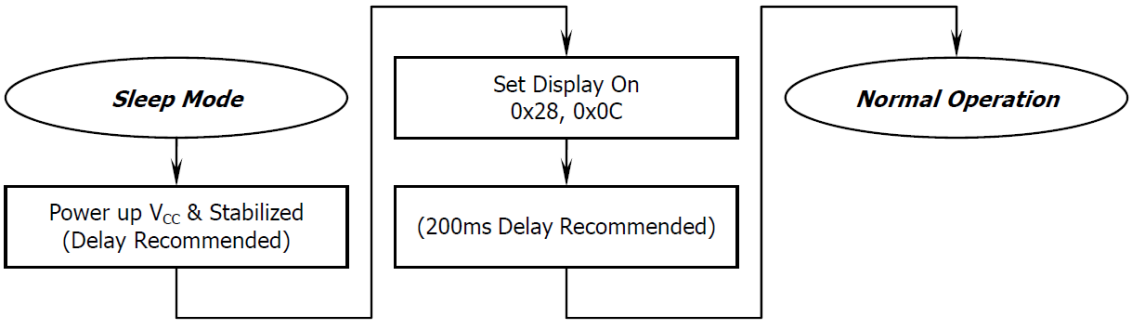
<Power down Sequence>



<Entering Sleep Mode>



<Exiting Sleep Mode>



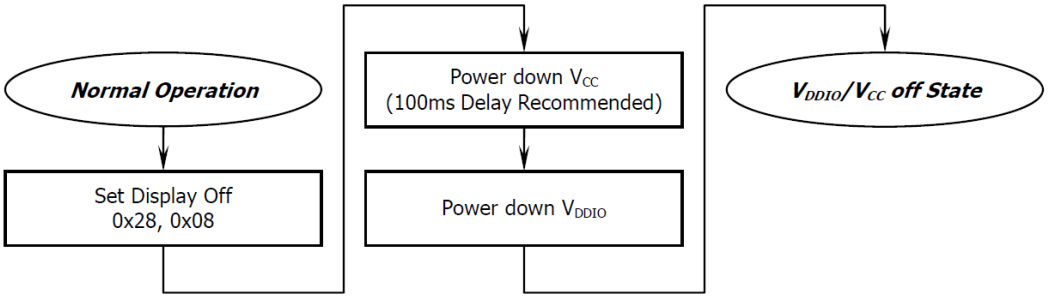
5.4.2 5V I/O Application

<Power up Sequence>

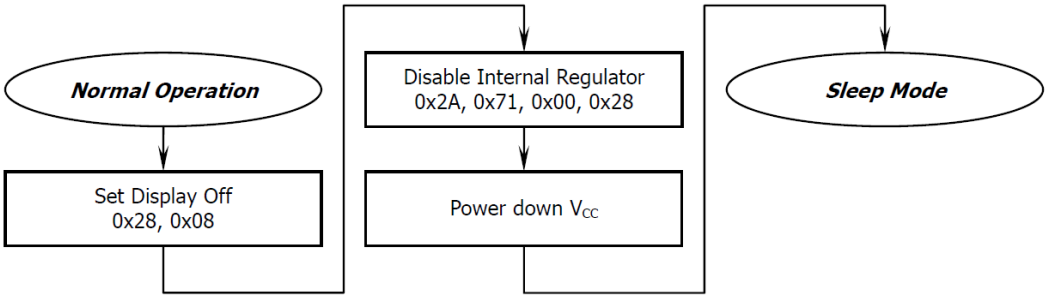
1) This command could be programmable or defined by pin configuration.
2) This command could be programmable or defined by pin configuration. The written value of the parameter should depend on the selection from Section 5.5

If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

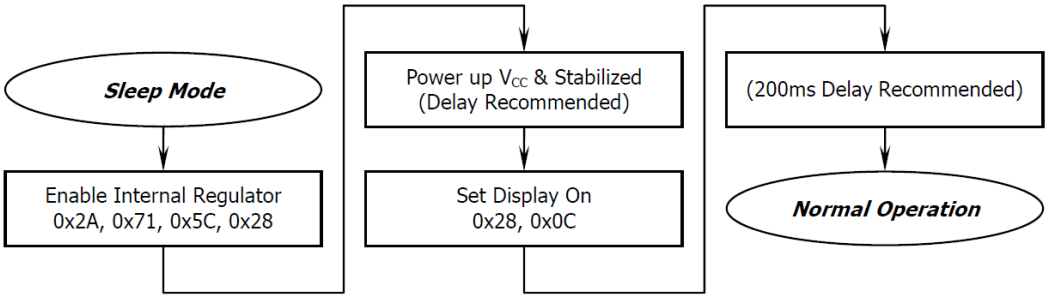
<Power down Sequence>



<Entering Sleep Mode>



<Exiting Sleep Mode>



5.5 US2066 CGROM CHARACTER CODE

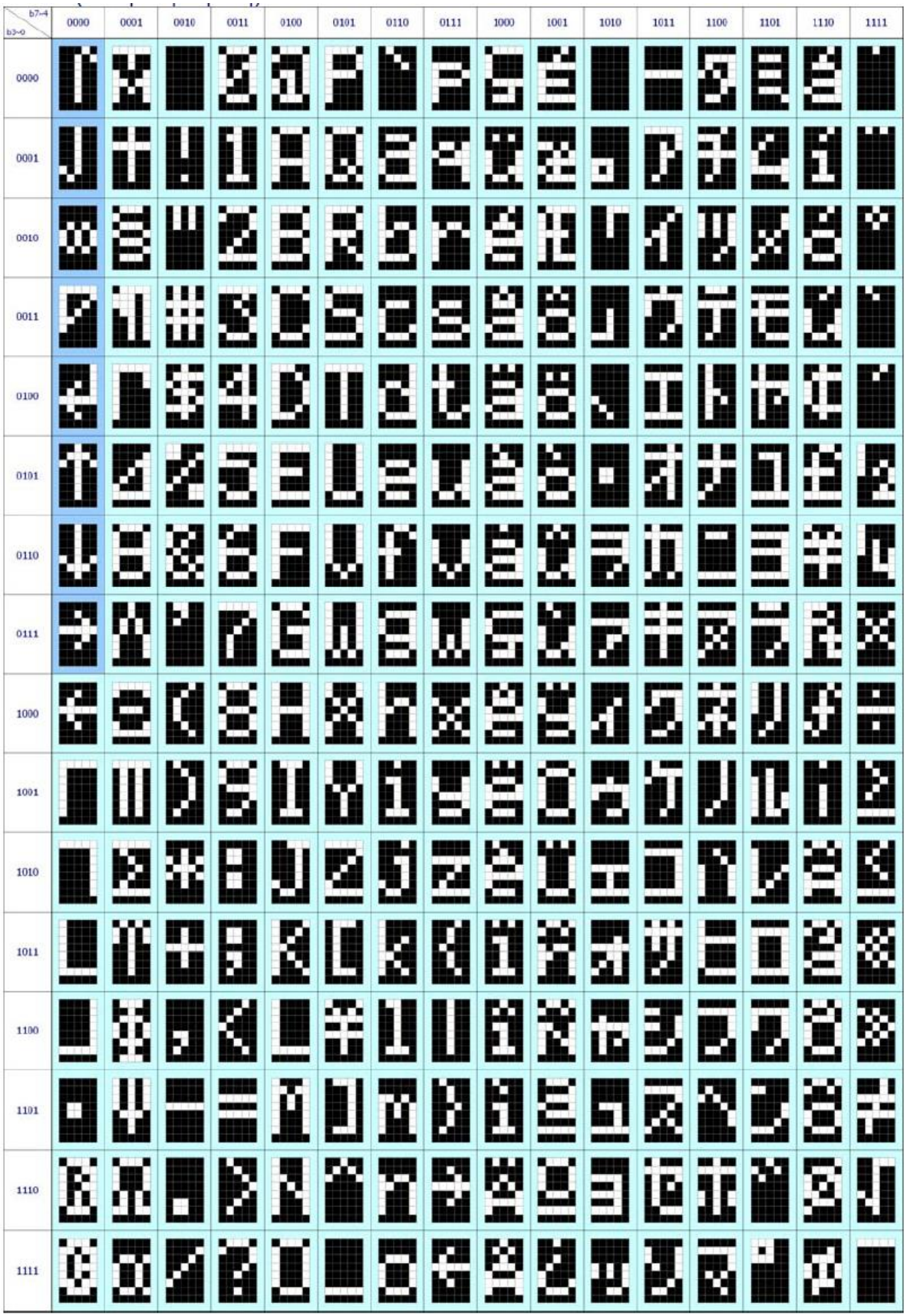
5.5.1 ROMA

Language: English, Irish, Spanish, Dutch (2), Danish, Norwegian, Swedish, Finnish, Czech (7), Slovene, Hungarian (2), Turkish (1)
The number in the parentheses is showing how many letters might be needed to build and define additionally at CGRAM. The darker background is showing the maximum addresses (00h~07h) those could be allocated by OPR [1:0] setting.

5.5.2 ROMB

Language: English, Irish, Portuguese, Spanish, French (1), Italian, German, Dutch (2), Icelandic, Danish, Norwegian, Swedish, Polish (8), Czech (8), Hungarian (2), Romanian (5), Turkish, Vietnamese (6), Russian (Small Letters)
The number in the parentheses is showing how many letters might be needed to build and define additionally at CGRAM. The darker background is showing the maximum addresses (00h~07h) those could be allocated by OPR[1:0] setting.

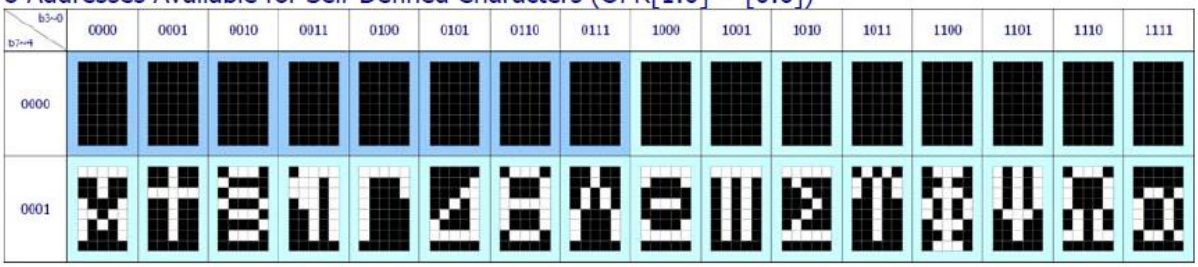
5.5.3 ROMC



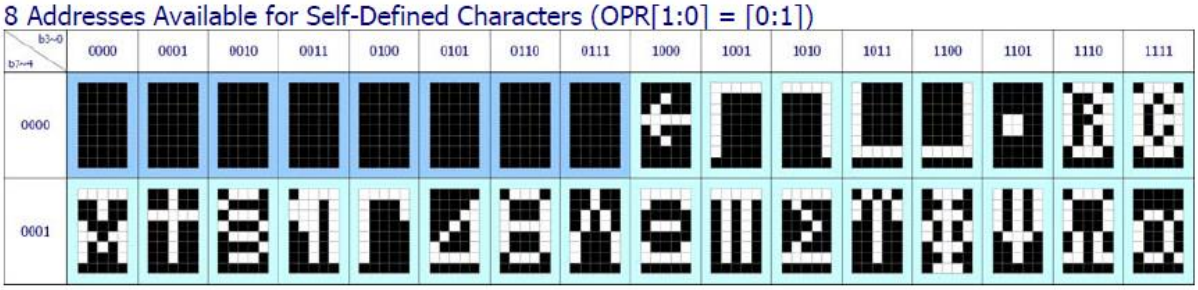
Language: English, Dutch (2), Japanese, Greek (Small Letters)
The number in the parentheses is showing how many letters might be needed to build and define additionally at CGRAM. The darker background is showing the maximum addresses (00h~07h) those could be allocated by OPR[1:0] setting.

5.6 SELF-DEFINED CGRAM (CHARACTER GENERATOR RAM)

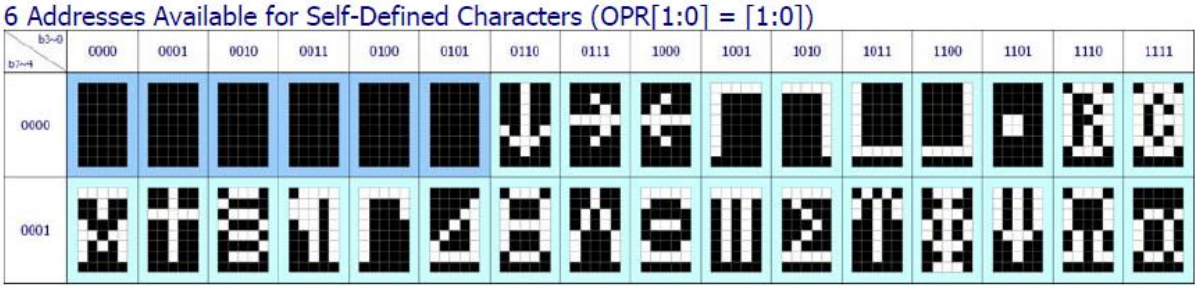
8 Addresses Available for Self-Defined Characters (OPR[1:0] = [0:0])



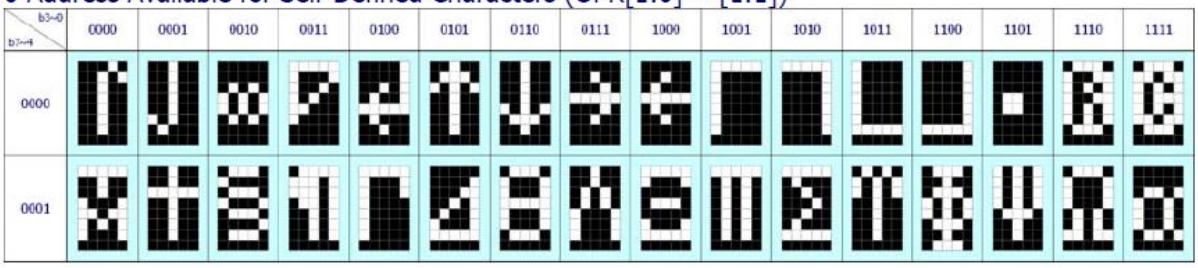
8 Addresses Available for Self-Defined Characters (OPR[1:0] = [0:1])



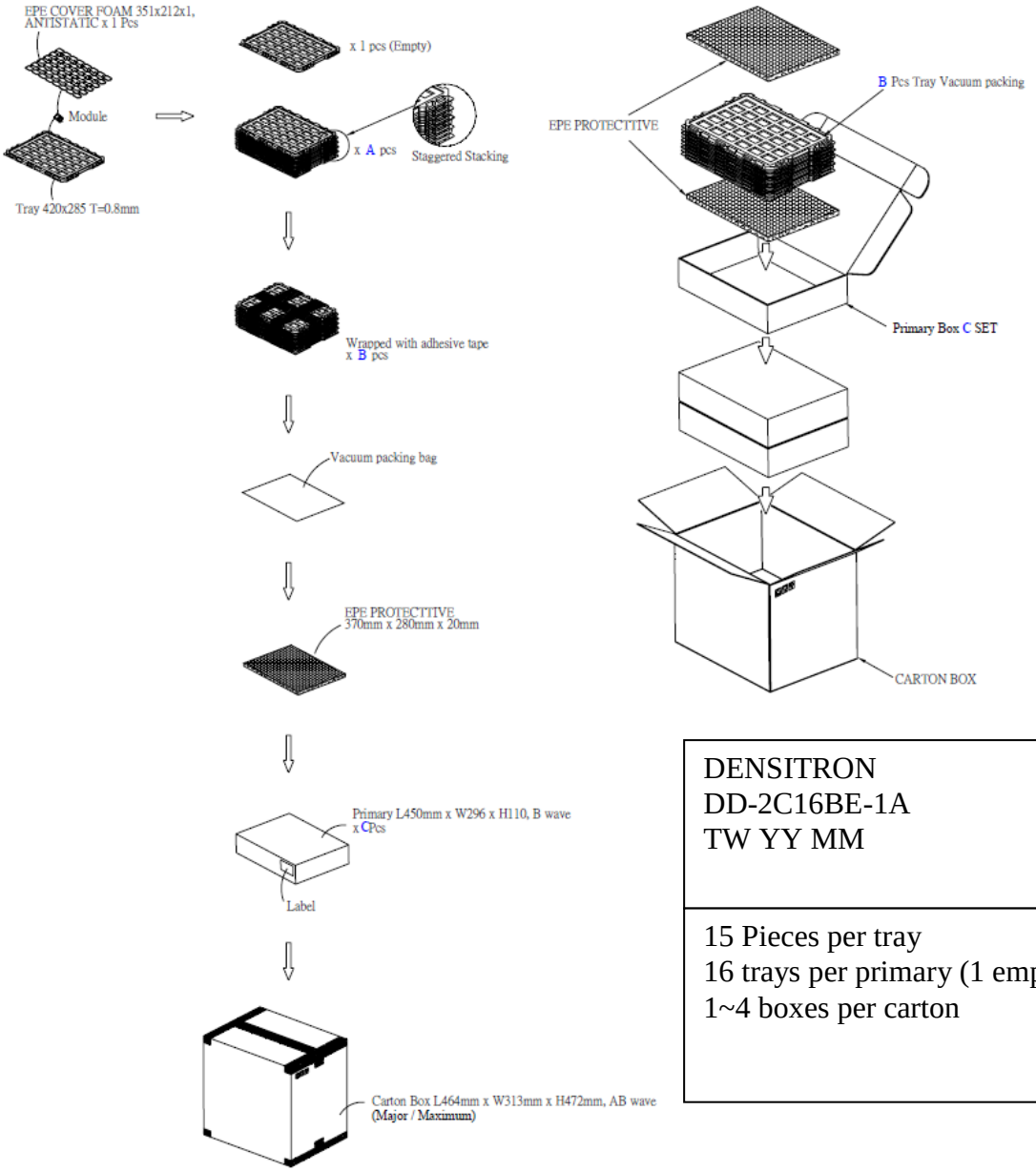
6 Addresses Available for Self-Defined Characters (OPR[1:0] = [1:0])



0 Address Available for Self-Defined Characters (OPR[1:0] = [1:1])



6 PACKAGING AND LABELLING SPECIFICATION



DENSITRON
DD-2C16BE-1A
TW YY MM

15 Pieces per tray
16 trays per primary (1 empty tray)
1~4 boxes per carton

7 QUALITY ASSURANCE SPECIFICATION

7.1 CONFORMITY

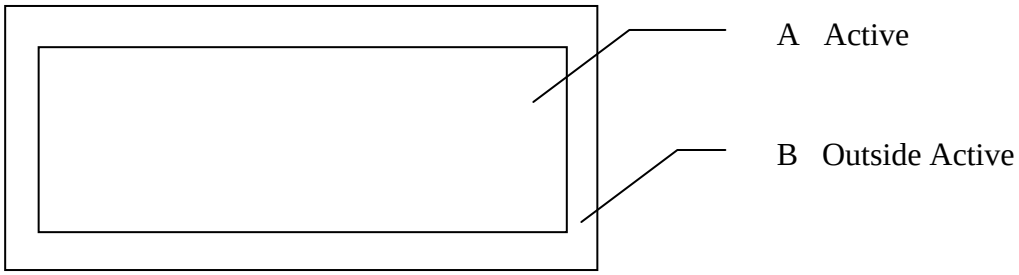
The performance, function and reliability of the shipped products conform to the Product Specification.

7.2 DELIVERY ASSURANCE

7.2.1 DELIVERY INSPECTION STANDARDS

IPC-AA610, class 2 electronic assemblies standard

7.2.2 Zone definition



7.2.3 Visual inspection

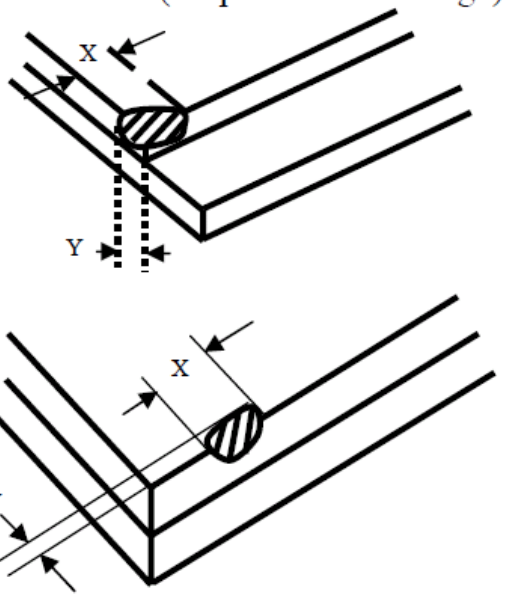
Test and measurement to be conducted under following conditions：

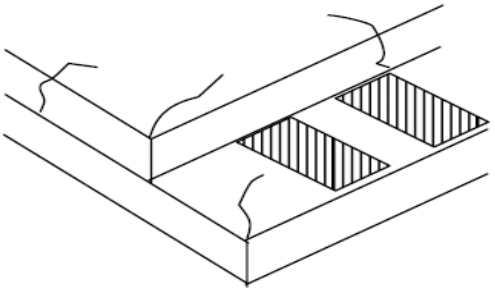
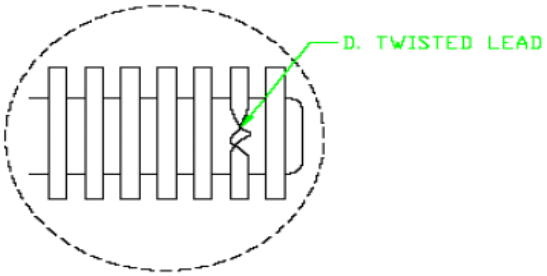
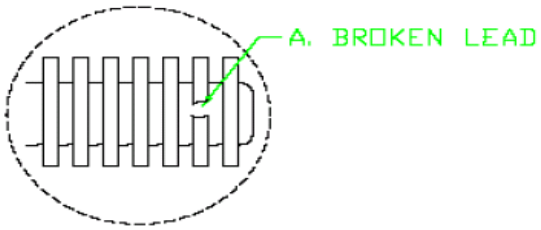
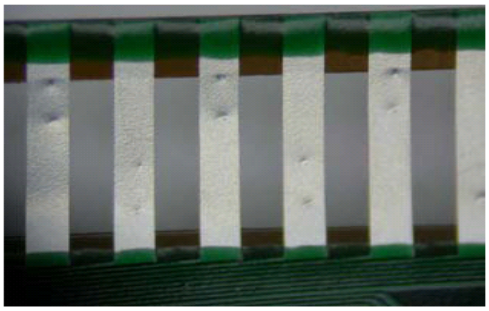
Temperature:	23±5℃
Humidity:	55±15%RH
Fluorescent lamp:	30 W
Distance between the Panel & Eyes of the Inspector:	≧30cm
Distance between the Panel & the lamp:	≧50cm

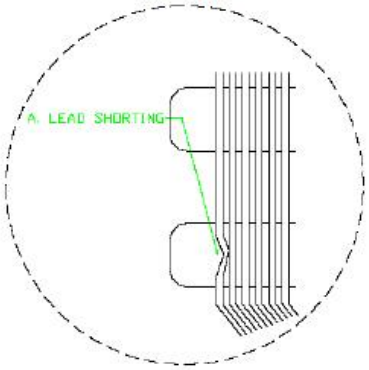
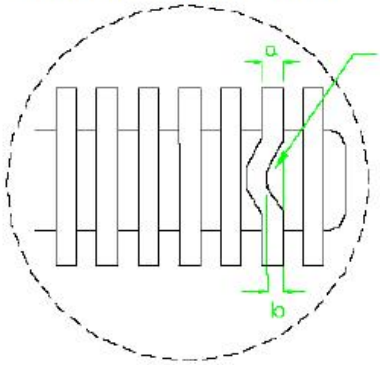
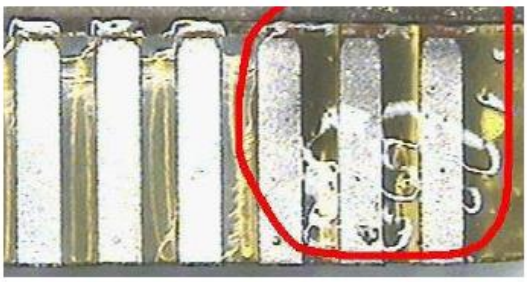
Finger glove (or finger cover) must be worn by the inspector.
Inspection table or jig must be anti-electrostatic

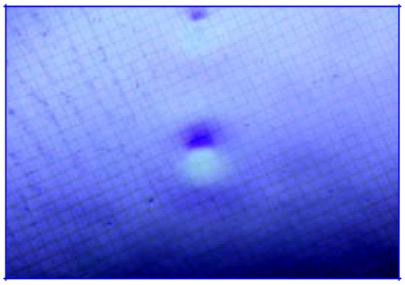
7.2.4 Standard of appearance inspection

Partition	AQL	Definition
Major	0.65	Defects in Pattern Check (Display On)
Minor	1.0	Defects in Cosmetic Check (Display Off)

Check Item	Classification	Criteria
Panel General Chipping	Minor	X > 6 mm (Along with Edge) Y > 1 mm (Perpendicular to edge) 

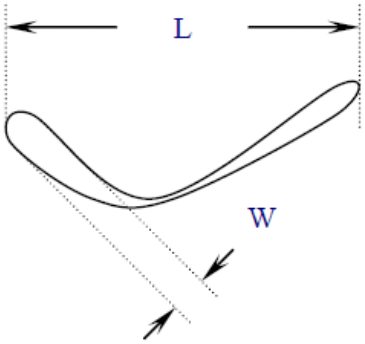
Check Item	Classification	Criteria
Panel Crack	Minor	Any crack is not allowable. 
Cupper Exposed (Even Pin or Film)	Minor	Not Allowable by Naked Eye Inspection
Film or Trace Damage	Minor	
Terminal Lead Twist	Minor	Not Allowable 
Terminal Lead Broken	Minor	Not Allowable 
Terminal Lead Prober Mark	Acceptable	

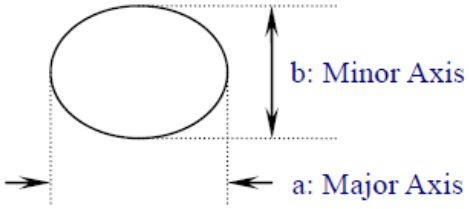
<table>
<tr><th>Check Item</th><th>Classification</th><th>Criteria</th></tr>
<tr><td rowspan="2">Terminal Lead Bent
(Not Twist or Broken)</td><td>Minor</td><td>NG if any bent lead cause lead shorting.
 
</td></tr>
<tr><td>Minor</td><td>NG for horizontally bent lead more than 50% of its width.
 
</td></tr>
<tr><td>Glue or Contamination on Pin
(Couldn’t Be Removed by Alcohol)</td><td>Minor</td><td>  </td></tr>
<tr><td>Ink Marking on Back Side of panel
(Exclude on Film)</td><td>Acceptable</td><td>Ignore for Any</td></tr>
</table>

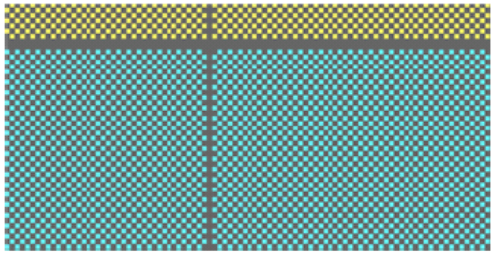
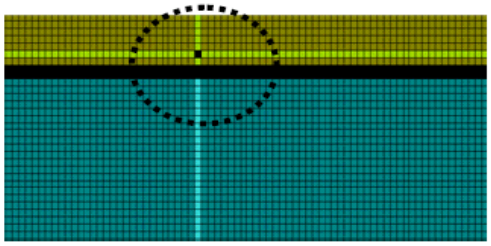
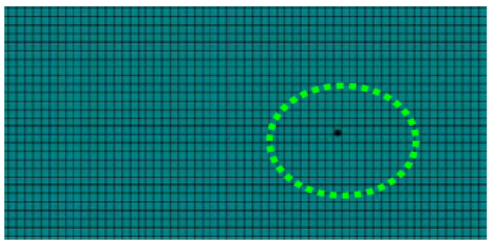
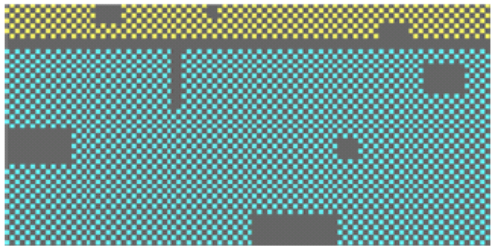
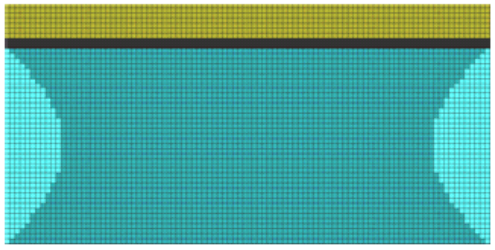
Check Item	Classification	Criteria
Any Dirt & Scratch on Polarizer's Protective Film	Acceptable	Ignore for not Affect the Polarizer
Scratches, Fiber, Line-Shape Defect (On Polarizer)	Minor	$W \le 0.1$ Ignore $W > 0.1, L \le 2$ $n \le 1$ $L > 2$ $n = 0$
Dirt, Black Spot, Foreign Material, (On Polarizer)	Minor	$\Phi \le 0.1$ Ignore $0.1 < \Phi \le 0.25$ $n \le 1$ $0.25 < \Phi$ $n = 0$
Dent, Bubbles, White spot (Any Transparent Spot on Polarizer)	Minor	$\Phi \le 0.5$ ➔ Ignore if no Influence on Display $0.5 < \Phi$ $n = 0$ 
Fingerprint, Flow Mark (On Polarizer)	Minor	Not Allowable

* Protective film should not be tear off when cosmetic check.

** Definition of W & L & Φ (Unit: mm): $\Phi = (a + b) / 2$





Check Item	Classification	Criteria
No Display	Major	
Flicker	Major	Not Allowable
Missing Line	Major	
Pixel Short	Major	
Darker Pixel	Major	
Wrong Display	Major	
Un-uniform	Major	

7.3 DEALING WITH CUSTOMER COMPLAINTS

7.3.1 Non-conforming analysis

Purchaser should supply Densitron with detailed data of non-conforming sample.
After accepting it, Densitron should complete the analysis in two weeks from receiving the sample.
If the analysis cannot be completed on time, Densitron must inform the purchaser.

7.3.2 Handling of non-conforming displays

If any non-conforming displays are found during customer acceptance inspection which Densitron is clearly responsible for, return them to Densitron.
Both Densitron and customer should analyse the reason and discuss the handling of non-conforming displays when the reason is not clear.
Equally, both sides should discuss and come to agreement for issues pertaining to modification of Densitron quality assurance standard.

8 RELIABILITY SPECIFICATION

8.1 RELIABILITY TESTS

Test Item	Test Condition	Evaluation and assessment
High Temperature Operation	80°C, 240 hours	No abnormalities in function and appearance
Low Temperature Operation	-40°C, 240 hours	No abnormalities in function and appearance
High Temperature Storage	90°C, 240 hours	No abnormalities in function and appearance
Low Temperature Storage	-40°C, 240 hours	No abnormalities in function and appearance
High Temperature & High Humidity Storage	60°C, 90%RH, 120 hours	No abnormalities in function and appearance
Thermal Shock	100 cycle of -40°C 1 Hour, 85°C 1 Hour. 60 Mins dwell	No abnormalities in function and appearance

- The samples used for above tests do not include polarizer.
- No moisture condensation is observed during tests.

8.1.1 FAILURE CHECK STANDARD

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure teat at 23±5 °C; 55±15% RH

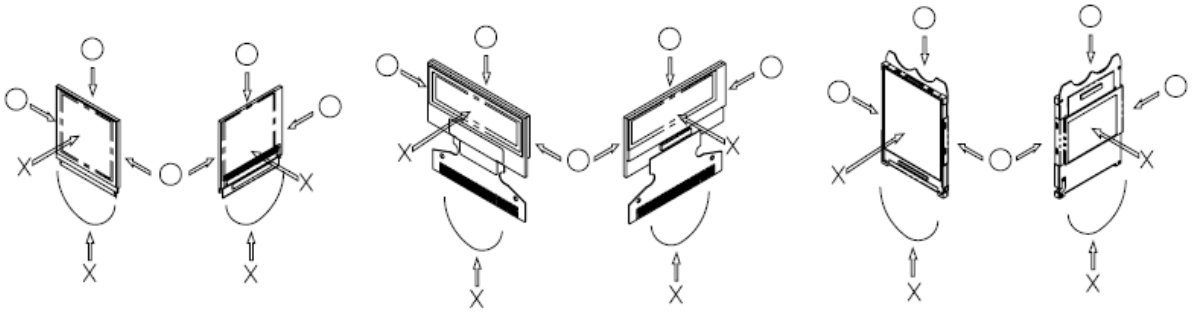
8.2 LIFE TIME

<table>
<tr><th>Item</th><th>Description</th></tr>
<tr><td>1</td><td>Function, performance, appearance, etc. shall be free from remarkable deterioration more than 15,000 hours under 80 cd/m² brightness and 50% Checkerboard, humidity (50% RH), and in area not exposed to direct sunlight. Software configuration follows Section 5.4 Initialization.
<table>
<tr><th>Parameter</th><th>Min</th><th>Max</th><th>Conditions</th></tr>
<tr><td>Life Time (80 cd/m2)</td><td>15,000</td><td>-</td><td rowspan="2">Vcc=9V, Ta=25°C, 50% Checkerboard.</td></tr>
<tr><td>Life Time (60 cd/m2)</td><td>25,000</td><td>-</td></tr>
</table>
</td></tr>
<tr><td>2</td><td>End of lifetime is specified as 50% of initial brightness. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.</td></tr>
</table>

9 HANDLING PRECAUTIONS

9.1 HANDLING PRECAUTIONS

1) Since the display panel is being made of glass, do not apply mechanical impacts such us dropping from a high position.
2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.
3) If pressure is applied to the display surface or its neighborhood of the OEL display module, the cell structure may be damaged and be careful not to apply pressure to these sections.
4) The polarizer covering the surface of the OEL display module is soft and easily scratched. Please be careful when handling the OEL display module.
5) When the surface of the polarizer of the OEL display module has soil, clean the surface. It takes advantage of by using following adhesion tape.
   * Scotch Mending Tape No. 810 or an equivalent
   Never try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy.
   Also, pay attention that the following liquid and solvent may spoil the polarizer:
   * Water
   * Ketone
   * Aromatic Solvents
6) Hold OEL display module very carefully when placing OEL display module into the system housing. Do not apply excessive stress or pressure to OEL display module. And, do not over bend the film with electrode pattern layouts. These stresses will influence the display performance. Also, secure sufficient rigidity for the outer cases.



7) Do not apply stress to the LSI chips and the surrounding molded sections.
8) Do not disassemble nor modify the OEL display module.
9) Do not apply input signals while the logic power is off.
10) Pay sufficient attention to the working environments when handing OEL display modules to prevent occurrence of element breakage accidents by static electricity.
    * Be sure to make human body grounding when handling OEL display modules.
    * Be sure to ground tools to use or assembly such as soldering irons.
    * To suppress generation of static electricity, avoid carrying out assembly work under dry environments.

* Protective film is being applied to the surface of the display panel of the OEL display module. Be careful since static electricity may be generated when exfoliating the protective film.

11) Protection film is being applied to the surface of the display panel and removes the protection film before assembling it. At this time, if the OEL display module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).
12) If electric current is applied when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

9.2 STORAGE PRECAUTIONS

1) When storing OEL display modules, put them in static electricity preventive bags avoiding exposure to direct sun light nor to lights of fluorescent lamps, etc. and, also, avoiding high temperature and high humidity environments or low temperature (less than 0°C) environments. (We recommend you to store these modules in the packaged state when they were shipped from Densitron Technologies Plc.) At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.
2) If electric current is applied when water drops are adhering to the surface of the OEL display module, when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

9.3 DESIGNING PRECAUTIONS

1) The absolute maximum ratings are the ratings which cannot be exceeded for OEL display module, and if these values are exceeded, panel damage may be happen.
2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the VIL and VIH specifications and, at the same time, to make the signal line cable as short as possible.
3) We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (VDD). (Recommend value: 0.5A)
4) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighboring devices.
5) As for EMI, take necessary measures on the equipment side basically.
6) When fastening the OEL display module, fasten the external plastic housing section.
7) If power supply to the OEL display module is forcibly shut down by such errors as taking out the main battery while the OEL display panel is in operation, we cannot guarantee the quality of this OEL display module.
8) The electric potential to be connected to the rear face of the IC chip should be as follows: US2066
   * Connection (contact) to any other potential than the above may lead to rupture of the IC.

9.4 OTHER PRECAUTIONS

1) When an OEL display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur. Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored. Also, there will be no problem in the reliability of the module.
2) To protect OEL display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the OEL display modules.
   * Pins and electrodes
   * Pattern layouts such as the FPC
3) With this OEL display module, the OEL driver is being exposed. Generally speaking, semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if this OEL driver is exposed to light, malfunctioning may occur.
   * Design the product and installation method so that the OEL driver may be shielded from light in actual usage.
   * Design the product and installation method so that the OEL driver may be shielded from light during the inspection processes.
4) Although this OEL display module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed. It therefore is necessary to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.
5) We recommend you to construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.

10 SUPPORTED ACCESSORIES

10.1 DUO KIT

Densitron has developed an easy to use yet powerful development and demonstration tool for driving its range of Passive Matrix OLED displays from the USB port of a PC.
DUO (Densitron USB OLED) kit is hot pluggable and does not require extra cables or power supply to run, allowing users to be up and running in minutes.

The kit consists of an OLED display with transition Board, USB controller card, mini USB cable and a CD with software application and drivers.

Part number: PDK-N-2C16BE-1A

10.2 TRANSITION BOARD CARD

A Transition board card is like a daughterboard which is meant to be a circuit board for connections between the baseboards (DUO).
It has connector pins for interfacing between the display and the baseboards.
It also includes the OLED display.
Part number: PDT-N-2C16BE-1A

10.3 CONNECTOR BOARD CARD

A Connector board card is also a daughterboard which is a circuit board for connection between a microprocessor or microcontroller (customer's system).
Part number: EVK-CONNECT-029

10.4 CONNECTOR

Type: hot bar soldering process
No. of connections: 33
Pitch: 0.70mm

10.5 APPLICATION NOTES AND EXAMPLE CODES

On request to Densitron