OLED DISPLAY MODULE

Product Specification

CUSTOMER	Standard	
PRODUCT NUMBER	DD-4C20WE-1A	
CUSTOMER APPROVAL		Date

INTERNAL APPROVALS		
Product Mgr	Doc. Control	Electr. Eng
Bazile Peter	**Luo Luo**	**Alan Wang**
Date: 26 Sep 12	Date: 26 Sep 12	Date: 26 Sep 12

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REVISION RECORD

Rev.	Date	Page	Chapt.	Comment	ECR no.
A	26 Sep 12			First Issue	
B	28 Nov 12	41	10	Update the connector information	

1 MAIN FEATURES

ITEM	CONTENTS
Characters x lines	20 x 4
Character Font	5 x 8
Overall Dimensions	84.50 x 27.50 x 2.00 mm
Colour	Monochrome White
Active Area	70.42 x 20.82 mm
Display Mode	Passive Matrix
Driving Method	1/32 duty
Driver IC	US2066
Operating temperature	-40 ~ +85
Storage temperature	-40 ~ +90

2 MECHANICAL SPECIFICATION

2.1 MECHANICAL CHARACTERISTICS

ITEM	CHARACTERISTIC	UNIT
Characters x lines	20 x 4	
Overall Dimensions	84.50 x 27.50 x 2.00	mm
Active Area	70.42 x 20.82	mm
Dot Size	0.57 x 0.57	mm
Dot Pitch	0.60 x 0.60	mm
Character size	2.97 x 4.77	mm
Weight	9.61	g
IC Controller/Driver	US2066	

Item	Date	Remark
A	20111108	Original Drawing
B	20120309	Add Double Side Tape On FPC

Segment 0 (Column 00)
Segment 50 (Column 50)
Common 0 (Row 0)
Common 31 (Row 31)
Segment 49 (Column 2)
Segment 99 (Column 1)
"A"

Detail "A"
Scale (2:1)

Pin	Symbol
1	N.C
2	VSL
3	VSS
4	REG VDD
5	SHLC
6	SHLS
7	VDD
8	VDDIO
9	RS0
10	RS1
11	RS2
12	GPIO
13	CS#
14	RES#
15	D/C#
16	R/W#(WR#)
17	E(RD#)
18	D0
19	D1
20	D2
21	D3
22	D4
23	D5
24	D6
25	D7
26	IREF
27	ROM0
28	ROM1
29	GPIO0
30	GPIO1
31	VCOMH
32	VCC
33	N.C

Densitron Displays

				Drawing Number	Rev.
				DMX2004SDGF02	B
				Material	
				Soda Lime / Polyimide	

Title	DD-4C 20WE-1A								
			Drawn	E.E.	Panel / E.	P.M.		Scale	1:1
By			Gary Lin	Ting Kuo Hu	Ivy Lo	Kate Chung		Sheet	1 of 1
Date			20120309	20120309	20120309	20120309		Size	A3

Customer Approval Signature

Unless Otherwise Specified

Unit	mm
General Roughness	

Tolerance	
Dimension	±0.3
Angle	±1

Active Area 2.89"
20 x 4 Character

(Reference Mechical Design)

Contact Side
Contact Side
3M Double Side Tape t=0.05mm
Protective Tape
Remove Tape t=0.15mm Max
Glue
Polarizer t=0.2mm

-13.75±0.3
-3.6±0.2
-1.8±0.3
-0.9
-0.1±0.03
(15)
2.5+0.1×0.1
W=0.4±0.03
-22±0.1 (Alignment Mark)
-P0.70x(33-1)=22.4±0.05
23.8±0.2
32.8
(7)
-10±0.3
S±0.05
8
5
10
(118.3)
-84.5±0.2 (Panel Size)
-80.5±0.2 (Cap Size)
-79.5 (Polarizer)
-72.42 (V/A)
-70.42 (A/A)
0.5±0.5
(4)
(5)
(3.34)
(2.34)
0.5±0.5
-20.82 (A/A)
-22.82 (V/A)
-26.5 (Polarizer)
-27.5±0.2 (Cap Size)
-27.5±0.2 (Panel Size)
2±0.1

-0.1±0.03
(0.15)
(1.84)
(2.2)
(31.08)
-3.55
-2.97
-0.58
0.6
0.57
-0.57
-0.6
-4.77
-5.35
-0.58

Notes:
1. Color: White
2. Driver IC: US2066
3. FPC Number: UT-0166-P01
4. Interface:
   4-/8-bit 68XX/80XX Parallel, SPI, I2C
5. General Tolerance: ±0.30
6. The total thickness (2.10 Max) is without polarizer protective film & remove tape.
   The actual assembled total thickness with above materials should be 2.35 Max.

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3 ELECTRICAL SPECIFICATION

3.1 ABSOLUTE MAXIMUM RATINGS

VSS = 0 V, Ta = 25 °C

Item	Symbol	Min	Max	Unit	Note
Supply Voltage for logic	V_{DD}	-0.3	6.0	V	
Supply Voltage for I/O Pins	V_{DDIO}	-0.3	6.0	V	Note 1, 2
Supply voltage for Display	V_{CC}	0	15	V	
Operating Temperature	T_{op}	-40	85	°C	Note 3
Storage Temperature	T_{st}	-40	90	°C	Note 3
Life Time (100 cd/m^2)		15,000	-	hour	Note 4
Life Time (80 cd/m^2)		30,000	-	hour	Note 4
Life Time (60 cd/m^2)		50,000	-	hour	Note 4

Note 1: All the above voltages are on the basis of "V_{SS}=0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent damage to the module may occur. Also for normal operations it's desirable to use this module under the conditions according to Section 3.2 "Electrical Characteristics". If this module is used beyond these conditions the module may malfunction and the reliability could deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80°C.

Note 4: V_{CC} =12.0V, Ta=25 °C, 50% Checkerboard.
Software configuration follows Section 5.4 Actual Application Example
End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

3.2 ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Logic	V_{DD}	5V I/O Application	-	-	-	V
		Low Voltage I/O Application	2.4	2.8	V_{DDIO}	V
Supply Voltage for I/O Pins	V_{DDIO}	5V I/O Application	4.4	5.0	5.5	V
		Low Voltage I/O Application	2.4	2.8	3.6	V
Supply Voltage for Display	V_{CC}	Note 1	11.5	12	12.5	V
High Level Input	V_{IH}	I_{OUT}=0.1mA, 3.3MHz	$0.8 \times V_{DDIO}$	-	V_{DDIO}	V
Low Level Input	V_{IL}		0	-	$0.2 \times V_{DDIO}$	V
High Level Output	V_{OH}	I_{OUT}=0.1mA, 3.3MHz	$0.9 \times V_{DDIO}$	-	V_{DDIO}	V
Low Level Output	V_{OL}		0	-	$0.1 \times V_{DDIO}$	V
Operating current for V_{DD}	I_{DD}	-	-	180	300	µA
Operating current for V_{CC}	I_{CC}	Note 2	-	14.1	17.6	mA
		Note 3	-	22.3	27.9	
		Note 4	-	43.3	54.1	
Sleep mode current for V_{DD}	I_{DD} SLEEP		-	1	10	µA
Sleep mode current for V_{CC}	I_{CC} SLEEP		-	2	10	µA

Note 1: Brightness (Lbr) and Supply Voltage for Display (VCC), are subject to the change of the panel characteristics

Note 2: V_{DD} = 2.8V, V_{CC} = 12.0V, 30% display area turned on.

Note 2: V_{DD} = 2.8V, V_{CC} = 12.0V, 50% display area turned on.

Note 4: V_{DD} = 2.8V, V_{CC} = 12.0V, 100% display area turned on.

* Software configuration follows section5.4 Actual Application Example.

3.3 INTERFACE PIN ASSIGNMENT

No.	Symbol	I/O	Function
1	N.C.(GND)	-	Reserved Pin (Supporting Pin) The supporting pin can reduce the influence from stress on the function pins. This pin must be connected to external ground as the ESD protection circuit.
2	VSL	P	Voltage Output Low Level for SEG signal This is segment voltage reference pin. When external V_{SL} is not used, this pin should be left open. When external V_{SL} is used, this pin should connect with resistor and diode to ground.
3	VSS	P	Ground of OEL System This is a ground pin. It also acts as a reference for the logic pins, the OEL driving voltages and the analogue circuits. It must be connected to external ground.
4	REGVDD	I	5V I/O Regulator Configuration This is internal V_{DD} regulator selection pin in 5V I/O application mode. When this pin is pulled LOW, internal V_{DD} regulator is disabled (Low Voltage I/O application). When this pin is pulled HIGH, internal V_{DD} regulator is enabled (5V I/O application).
5	SHLC	I	Scanning Direction for COM signal This pin is used to determine the COM output scanning direction. It can still be programmable and defined by fundamental command.
6	SHLS	I	Mapping Direction for SEG Selection This pin is used to change the mapping between the display data column address and the segment driver. It can still be programmable and defined by fundamental command.
7	VDD	P	Power Supply for Logic Circuit This is a voltage supply pin which is supplied externally or regulated internally. A capacitor should be connected between this pin and Vss under all circumstances. When internal V_{DD} is disabled, this is a power input pin. It must be connected to V_{DDIO} or external source and always be equal to or lower than V_{DDIO}. (Low Voltage I/O Application) When internal V_{DD} is enabled, it is regulated internally from V_{DDIO}. (5V I/O Application)
8	VDDIO	P	Power Supply for Interface Logic Level This is a voltage supply pin. It should match with the MCU interface voltage level and must be connected to external source.
9	BS0	I	Communicating Protocol Selection These pins are MCU interface selection input. See the following table:
10	BS1		

	BS0	BS1	BS2
I^2C	0	1	0
Serial	0	0	0
4-bit 68XX-Parallel	1	0	1

11	BS2		4-bit 80XX-Parallel	1	1	1
			8-bit 68XX-Parallel	0	0	1
			8-bit 68XX-Parallel	0	1	1

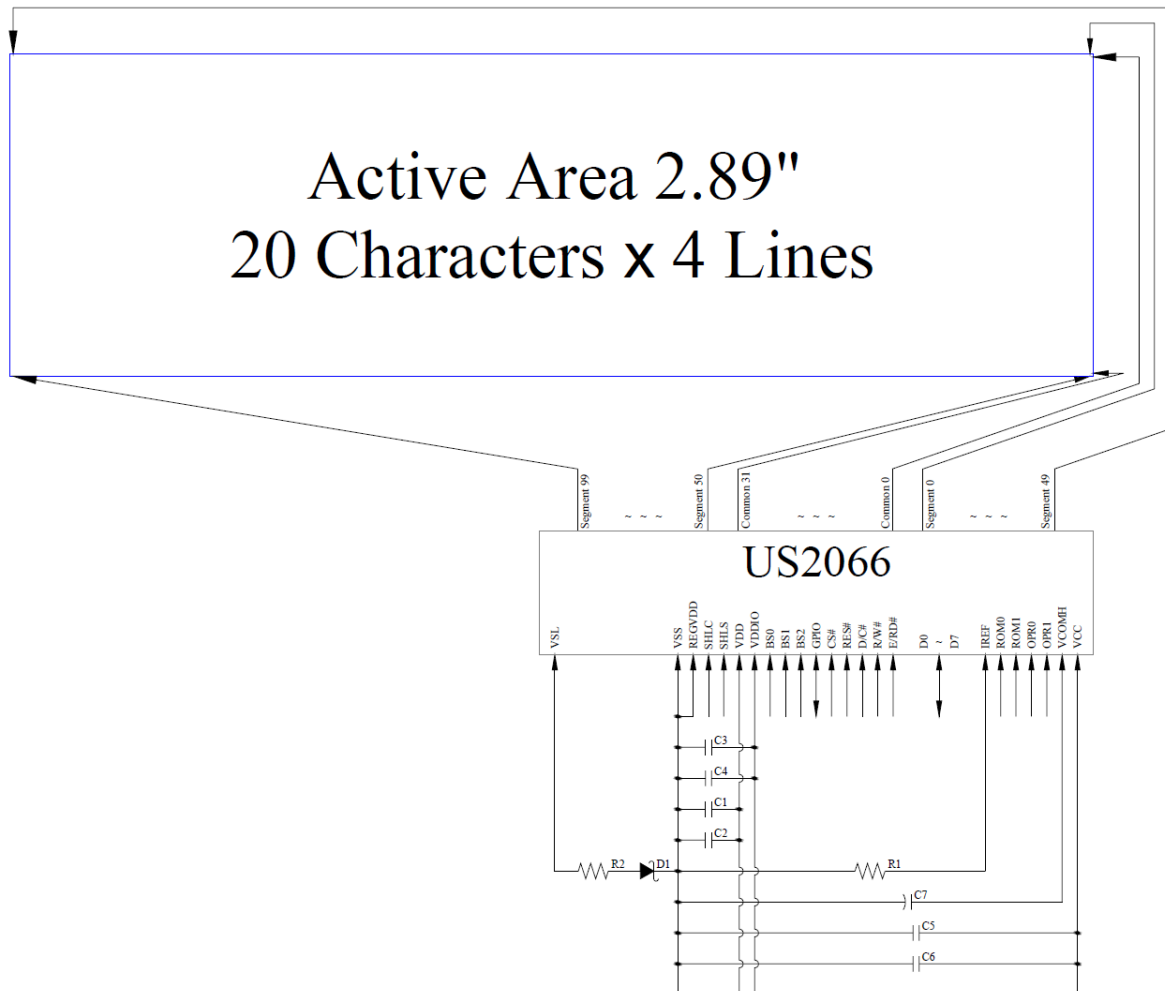| 12	GPIO	I/O	**General Purpose Input/Output** This pin could be left open individually or have signal inputted/outputted. It is able to use as the external DC/DC converter circuit enabled/disabled control or other applications.
13	CS#	I	**Chip Select** This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.
14	RES#	I	**Power Reset for Controller and Driver** This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation.
15	D/C#	I	**Data/Command Control** This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 will be interpreted as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register. In I2C mode, this pin acts as SA0 for slave address selection. When serial interface mode is selected, this pin must be connected to VSS. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.
16	R/W#	I	**Read/Write Select or Write** This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to "High" for read mode and pull it to "Low" for write mode. When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low. When serial or I2C mode is selected, this pin must be connected to V_{SS}.
17	E/RD#	I	**Read/Write Enable or Read** This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low. When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low. When serial or I^2C mode is selected, this pin must be connected to V_{SS}.
18~25	D0~D7	I/O	**Host Data Input/Output Bus** These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D0 will be the serial clock input SCLK; D1 will be the serial data input SID and D2 will be the serial clock output SOD. When I2C mode is selected, D2, D1 should be tired together and serve as SDAOUT, SDAIN in application and D0 is the serial clock input, SCL. Unused pins must be connected to VSS.

26	IREF	I	**Current Reference for Brightness Adjustment** This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current at 15uA.
27	ROM0	I	**Built-in Character ROM Selection** These pins are used to select Character ROM. See the following table:
28	ROM1		
29	OPR0	I	**Character ROM/RAM Management** These pins are used to manage the character number of character generator. See the following table:
30	OPR1		
31	VCOMH	P	**Voltage Output High Level for COM Signal** This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and V_{SS}.
32	VCC	P	**Power Supply for OEL Panel** This is the most positive voltage supply pin of the chip. It must be connected to external source.
33	N.C.(GND)	-	**Reserved Pin (Supporting Pin)** The supporting pin can reduce the influence from stress on the function pins. This pin must be connected to external ground as the ESD protection circuit.

Table for pins 27/28:

ROM	ROM0	ROM1
A	0	0
B	1	0
C	0	1
S/W selectable	1	1

It can still be programmable and defined by extended command.

Table for pins 29/30:

CGROM	CGRAM	OPR0	OPR1
240	8	0	0
248	8	1	0
250	6	0	1
256	0	1	1

It can still be programmable and defined by extended command.

3.4 BLOCK DIAGRAM
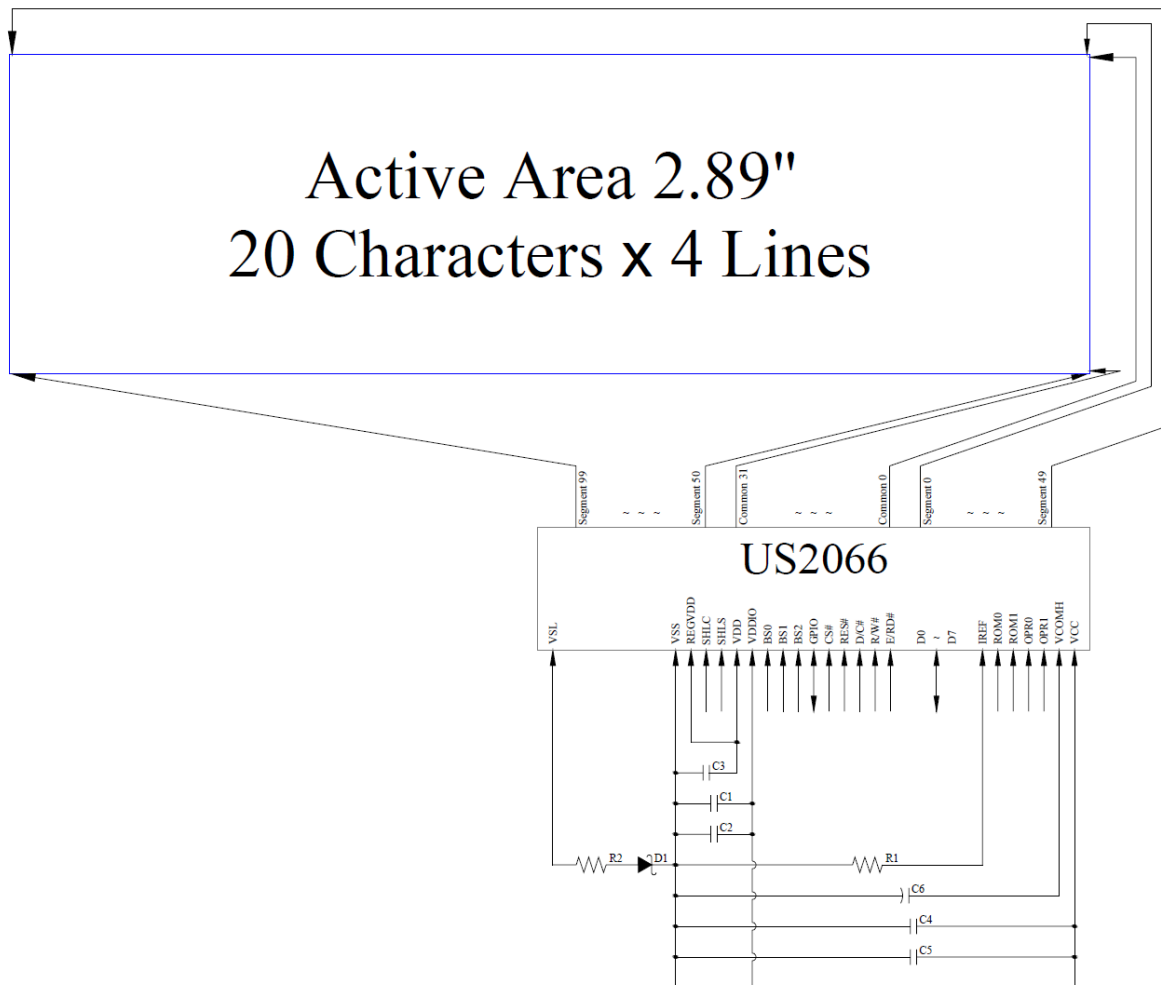
3.4.1 Low Voltage I/O Application

MCU Interface Selection: BS0, BS1 and BS2
Pins connected to MCU interface: CS#, RES#, D/C#, R/W#, E/RD#, and D0~D7
* SHLC, SHLC, ROM0, ROM1, OPR0 and OPR1 should be configured.

C1, C3, C5: 0.1µF
C2, C4:   4.7µF
C6:   10µF
C7:   4.7µF / 25V Tantalum Capacitor
R1:   470kΩ, R1 = (Voltage at IREF - VSS) / IREF
R2:   50Ω, 1/4W
D1:   ≤1.4V, 0.5W

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3.4.2 5V I/O Application

MCU Interface Selection: BS0, BS1 and BS2
Pins connected to MCU interface: CS#, RES#, D/C#, R/W#, E/RD#, and D0~D7
* SHLC, SHLC, ROM0, ROM1, OPR0 and OPR1 should be configured.

C1, C4: 0.1µF
C2:   4.7µF
C3:   1µF
C5:   10µF
C6:   4.7µF / 25V Tantalum Capacitor
R1:   470kΩ, R1 = (Voltage at IREF - VSS) / IREF
R2:   50Ω, 1/4W
D1:   ≤1.4V, 0.5W

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3.5 TIMING CHARACTERISTICS

3.5.1 AC CHARACTERISTICS

3.5.1.1 68XX-Series MPU Parallel Interface Timing Characteristics

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time (Write Cycle)	400	-	ns
t_{AS}	Address Setup Time	13	-	ns
t_{AH}	Address Hold Time	17	-	ns
t_{DSW}	Write Data Setup Time	35	-	ns
t_{DHW}	Write Data Hold Time	18	-	ns
t_{DHR}	Read Data Hold Time	13	-	ns
t_{OH}	Output Disable Time	10	90	ns
t_{ACC}	Access Time (RAM)	-	125	ns
	Access Time (Command)			
t_{CS}	Chip Select Time	0	-	ns
t_{CH}	Chip Select Hold Time	0	-	ns
PW_{CSL}	Chip Select Low Pulse Width (Read RAM)	250	-	ns
	Chip Select Low Pulse Width (Read Command)	250		
	Low Pulse width (Write)	50		
PW_{CSH}	Chip Select High Pulse Width (Read) Chip Select	155	-	ns
	High Pulse Width (Write)	55		
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

*(V_{DDIO} - V_{SS} = 2.4V to 3.6V/4.4V to 5.5V, T_a = 25 ºC)

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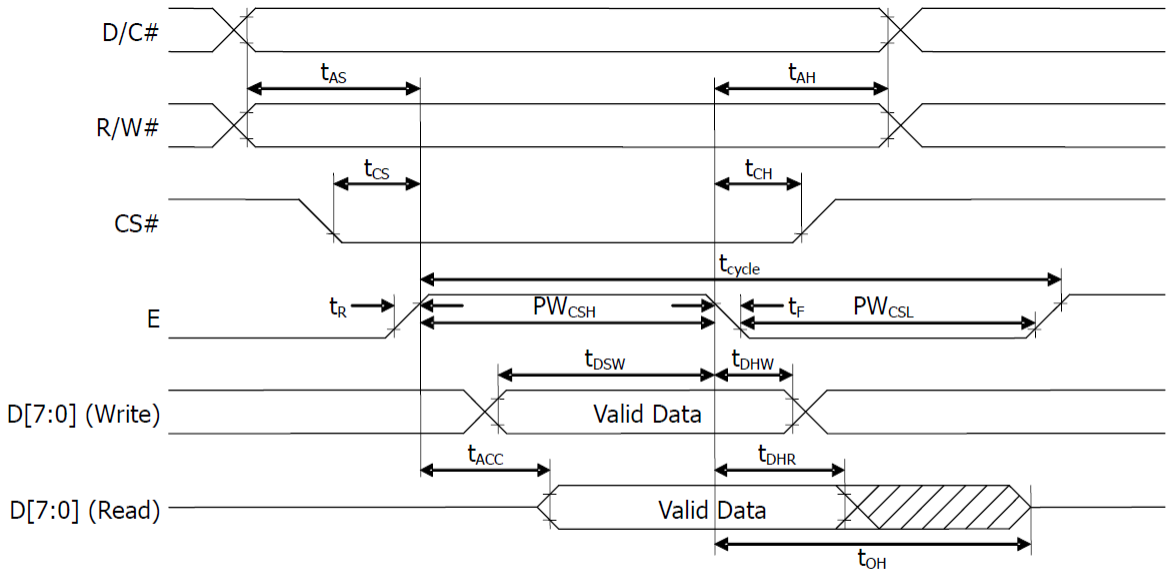
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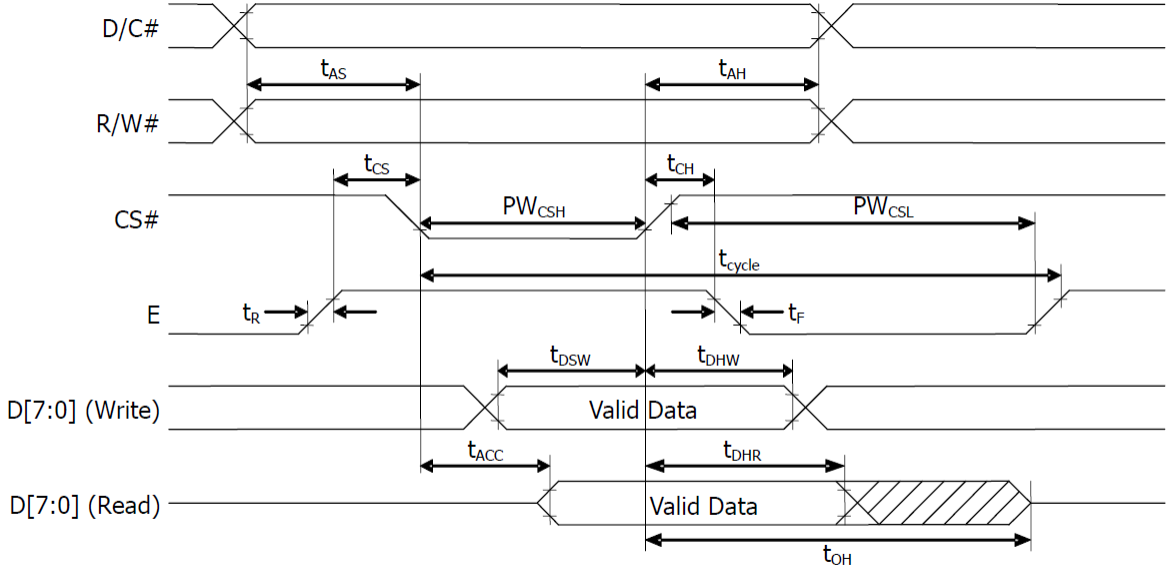
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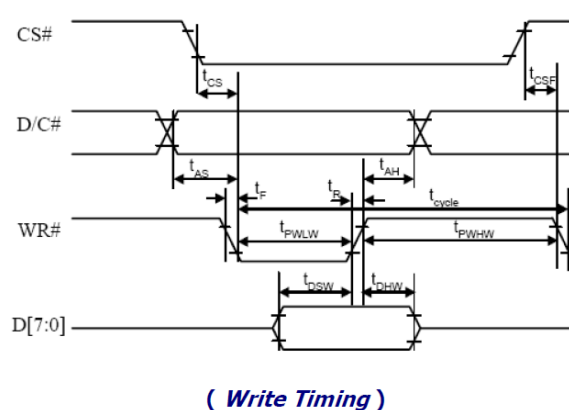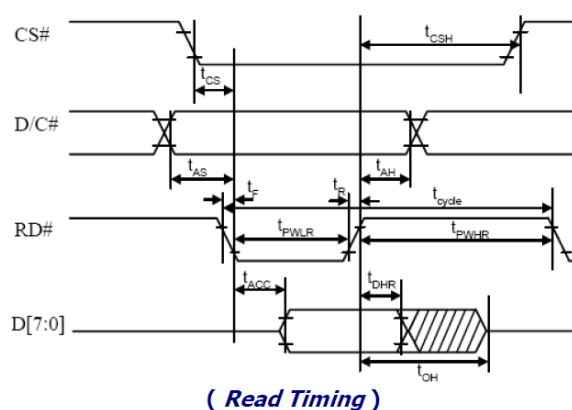
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3.5.1.2 80XX-Series MPU Parallel Interface Timing Characteristics

VDDIO-VSS = 2.4V to 3.6V/4.4V to 5.5V, Ta = 25°C

Symbol	Description	Min	Max	Unit
t_{cycle}	System Cycle Time	400	-	ns
t_{AS}	Address Setup Time	13	-	ns
t_{AH}	Address Hold Time	17	-	ns
t_{DSW}	Write Data Setup Time	35	-	ns
t_{DHW}	Write Data Hold Time	18	-	ns
t_{DHR}	Read Data Hold Time	13	-	ns
t_{OH}	Output Disable Time	10	70	ns
t_{ACC}	Access Time (RAM)	-	125	ns
	Access Time (Command)			
t_{CS}	Chip Select Time	0	-	ns
t_{CSH}	Chip Select Hold Time to Read Signal	0	-	ns
t_{CSF}	Chip Select Hold Time	0	-	ns
PW_{CSL}	Chip Select Low Pulse Width (Read RAM)- t_{PWLR}	250	-	ns
	Chip Select Low Pulse Width (Read Command)- t_{PWLR}	250		
	Low Pulse width (Write)- t_{PWLW}	50		
PW_{CSH}	Chip Select High Pulse Width (Read)- t_{PWHR}	155	-	ns
	High Pulse Width (Write)- t_{PWHW}	55		
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

(*Read Timing*)   (*Write Timing*)

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3.5.1.3 Serial Interface Timing Characteristics

Symbol	Description	Min	Max	Unit
t_{cycle}	Serial Clock Cycle Time	1	20	ns
t_{su1}	Chip Select Setup Time	60	-	ns
t_{h1}	Chip Select Hold Time	20	-	ns
t_{su2}	Serial Input Data Setup Time	200	-	ns
t_{h2}	Serial Input Data Hold Time	TBD	-	ns
t_D	Serial Output Data Delay Time	-	TBD	ns
t_{DH}	Serial Output Data Hold Time	10	-	ns
t_W	Serial Clock Width (Low, High)	400	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

$^*(V_{DDIO} - V_{SS} = 2.4V$ to $3.6V/4.4V$ to $5.5V$, $T_a = 25\ ^oC)$
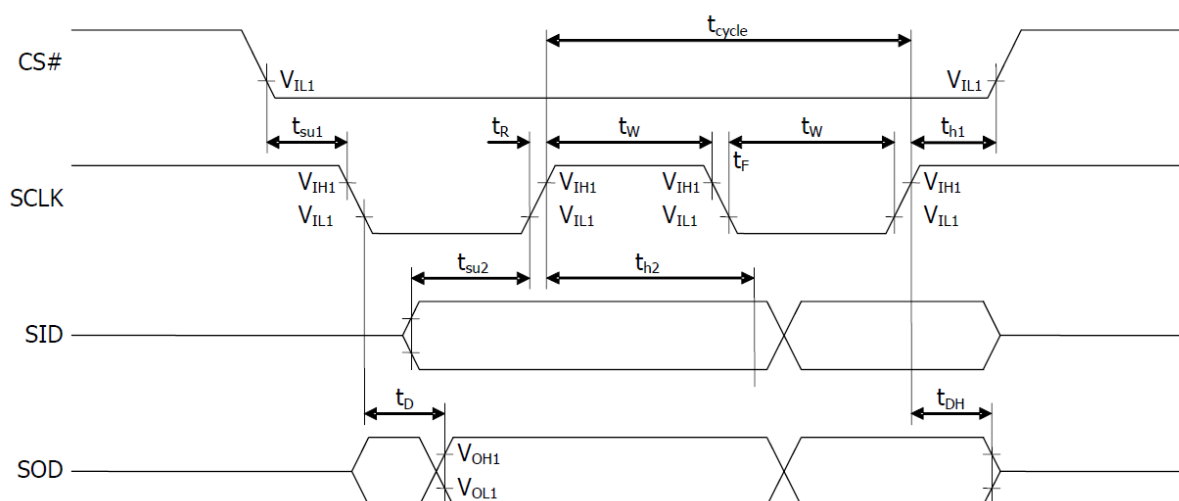
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3.5.1.4 I²C Interface Timing Characteristics

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	us
t_{HSTART}	Start Condition Hold Time	0.6	-	us
t_{HD}	Data Hold Time (for "SDAOUT" Pin) Data	5	-	ns
	Hold Time (for "SDAIN" Pin)	300		
t_{SD}	Data Setup Time	100	-	ns
t_{SSTART}	Start Condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	us
t_{SSTOP}	Stop Condition Setup Time	0.6	-	us
t_R	Rise Time for Data and Clock Pin		300	ns
t_F	Fall Time for Data and Clock Pin		300	ns
t_{IDLE}	Idle Time before a New Transmission can Start	1.3	-	us

*(V_{DDIO} - V_{SS} = 2.4V to 3.6V/4.4V to 5.5V, T_a = 25 ºC)
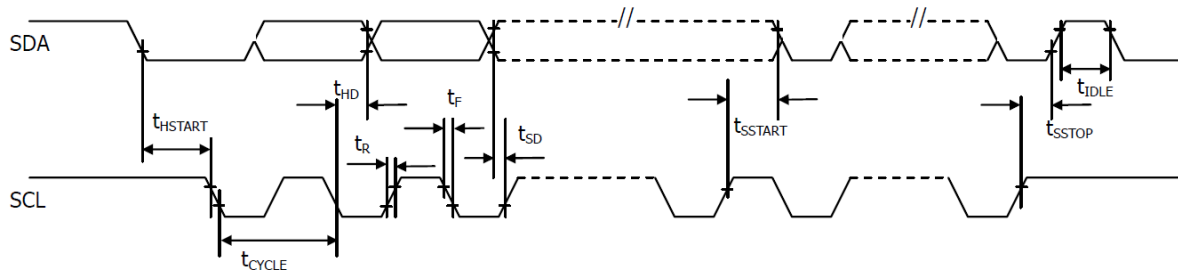
4 OPTICAL SPECIFICATION

4.1 OPTICAL CHARACTERISTICS

Characteristics	Symbol	Condition	Min	Typ	Max	Unit
Brightness	L_{br}	Note 1	80	100	-	cd/m^2
C.I.E.(White)	(X)	C.I.E. 1931	0.25	0.29	0.33	-
	(Y)		0.27	0.31	0.35	
Dark Room Contrast	CR		-	>10,000:1	-	-
Viewing Angle			-	Free	-	degree

Optical measurement taken at V_{DD} = 2.8V or 5.0V, V_{CC} = 12.0V.
Software configuration follows Section 5.4 Actual Application Example

Note 1 Brightness (L_{br}) and Supply Voltage for Display (V_{CC}) are subject to the change of the panel characteristics and the customers request

5 FUNCTIONAL SPECIFICATION

5.1 COMMANDS

Please refer to the Technical Manual for the US2066

5.2 POWER UP/DOWN SEQUENCE

To protect panel and extend the panel lifetime, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the panel enough time to complete the action of charge and discharge before/after the operation.
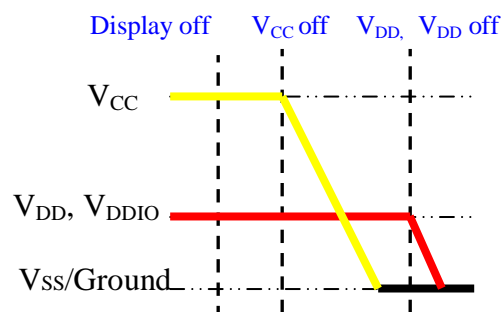
5.2.1 POWER UP SEQUENCE

1. Power up V_{DD} and V_{DDIO}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{CC}
6. Delay 100ms
(When Vcc is stable)
7. Send Display on command
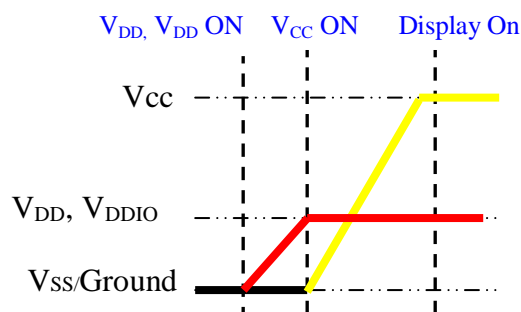
5.2.2 POWER DOWN SEQUENCE

1. Send Display off command
2. Power down V_{CC}
3. Delay 100ms
   (When V_{cc} reaches 0 and panel is
   Completely discharged)
4. Power down V_{DD} and V_{DDIO}

Conditions:

1) Since an ESD protection circuit is connected between V_{DD}, V_{DDIO} and V_{CC} inside the driver IC, V_{CC} becomes lower than V_{DD} & V_{DDIO} whenever V_{DD} & V_{DDIO} is ON and V_{CC} is OFF.
2) V_{CC} should be kept float (disable) when it is OFF.
3) Power Pins (V_{DD}, V_{DDIO}, V_{CC}) can never be pulled to ground under any circumstance.
4) V_{DD} & V_{DDIO} should not be power down before V_{CC} power down.

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5.3 RESET CIRCUIT

When RES# input is low, the chip is initialized with the following status:
1. Display is off
2. 5X8 Character Mode
3. Display start position is set at display RAM address 0
4. CGRAM address counter is set at 0
5. Cursor is OFF
6. Blink is OFF
7. Contrast control register is set at 7Fh
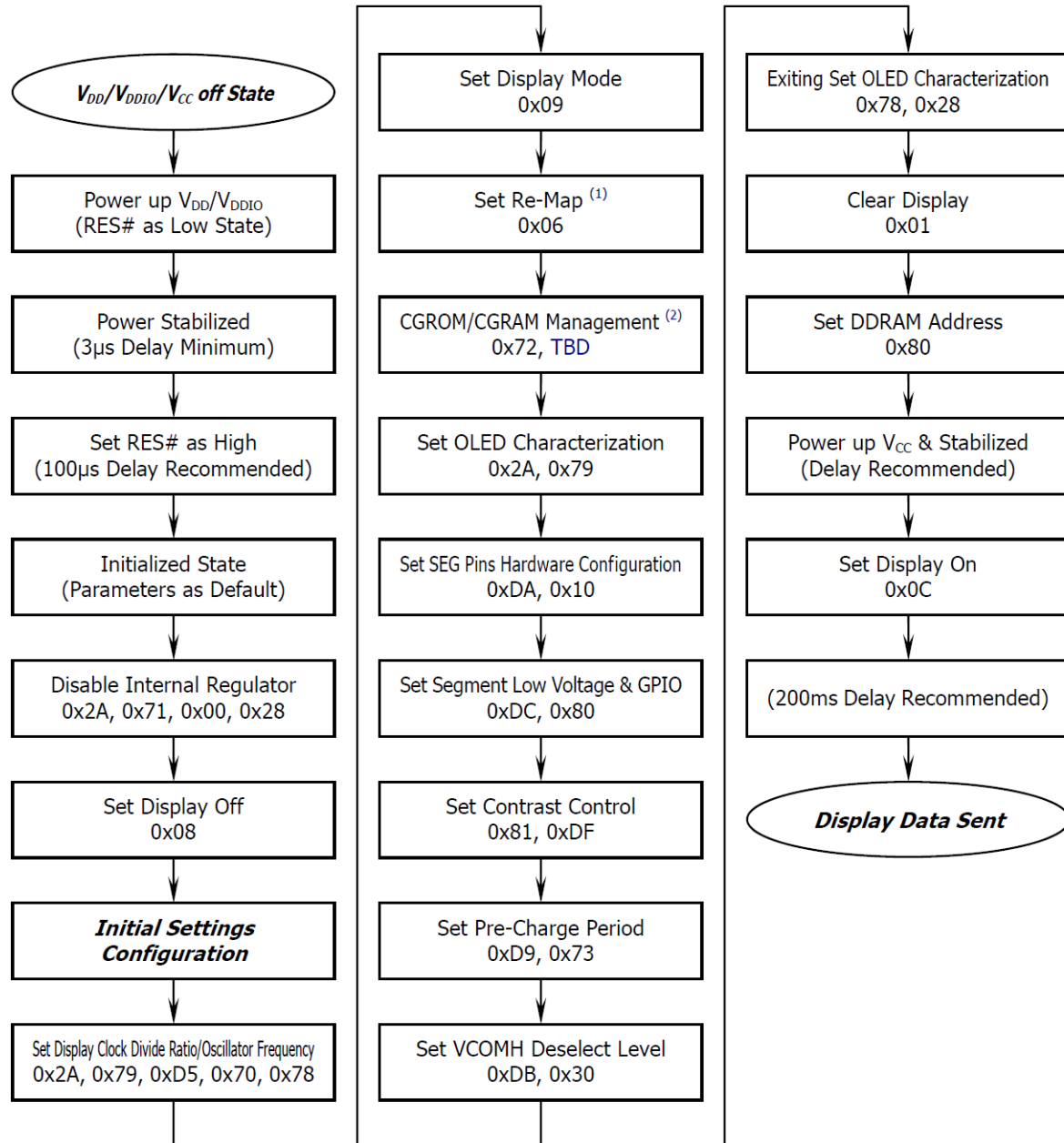8. OLED command set is disabled

5.4 ACTUAL APPLICATION EXAMPLE

Command usage and explanation of an actual example

5.4.1 Low Voltage I/O Application

Column 1:

$V_{DD}/V_{DDIO}/V_{CC}$ **off State**

↓

Power up V_{DD}/V_{DDIO}
(RES# as Low State)

↓

Power Stabilized
(3μs Delay Minimum)

↓

Set RES# as High
(100μs Delay Recommended)

↓

Initialized State
(Parameters as Default)

↓

Disable Internal Regulator
0x2A, 0x71, 0x00, 0x28

↓

Set Display Off
0x08

↓

Initial Settings Configuration

↓

Set Display Clock Divide Ratio/Oscillator Frequency
0x2A, 0x79, 0xD5, 0x70, 0x78

Column 2:

Set Display Mode
0x09

↓

Set Re-Map [1]
0x06

↓

CGROM/CGRAM Management [2]
0x72, TBD

↓

Set OLED Characterization
0x2A, 0x79

↓

Set SEG Pins Hardware Configuration
0xDA, 0x10

↓

Set Segment Low Voltage & GPIO
0xDC, 0x80

↓

Set Contrast Control
0x81, 0xDF

↓

Set Pre-Charge Period
0xD9, 0x73

↓

Set VCOMH Deselect Level
0xDB, 0x30

Column 3:

Exiting Set OLED Characterization
0x78, 0x28

↓

Clear Display
0x01

↓

Set DDRAM Address
0x80

↓

Power up V_{CC} & Stabilized
(Delay Recommended)

↓

Set Display On
0x0C

↓

(200ms Delay Recommended)

↓

Display Data Sent

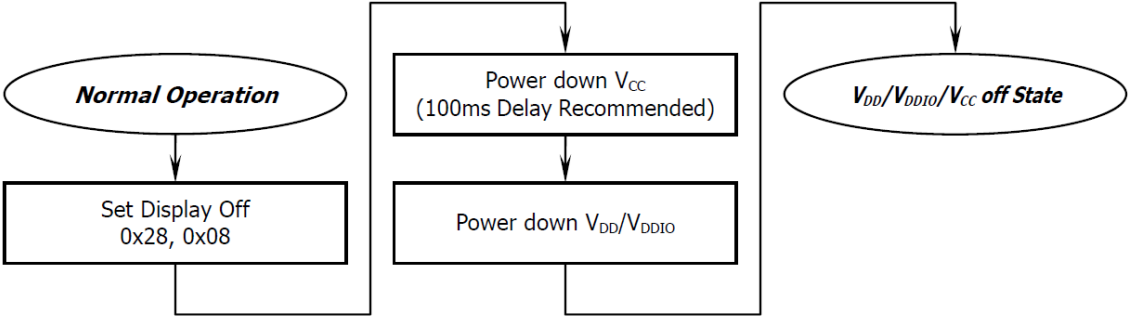(1) This command could be programmable or defined by pin configuration.
(2) This command could be programmable or defined by pin configuration. The written value of the parameter should depend on the selection from section 5.5 and 5.6

If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.
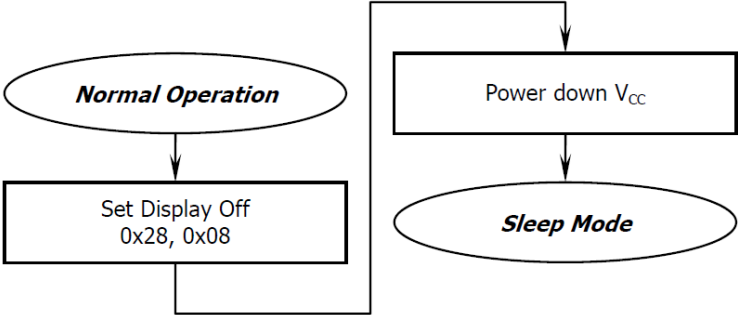
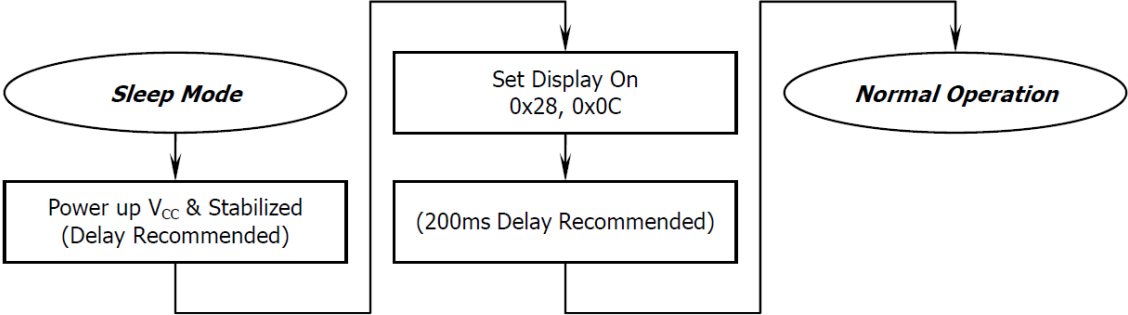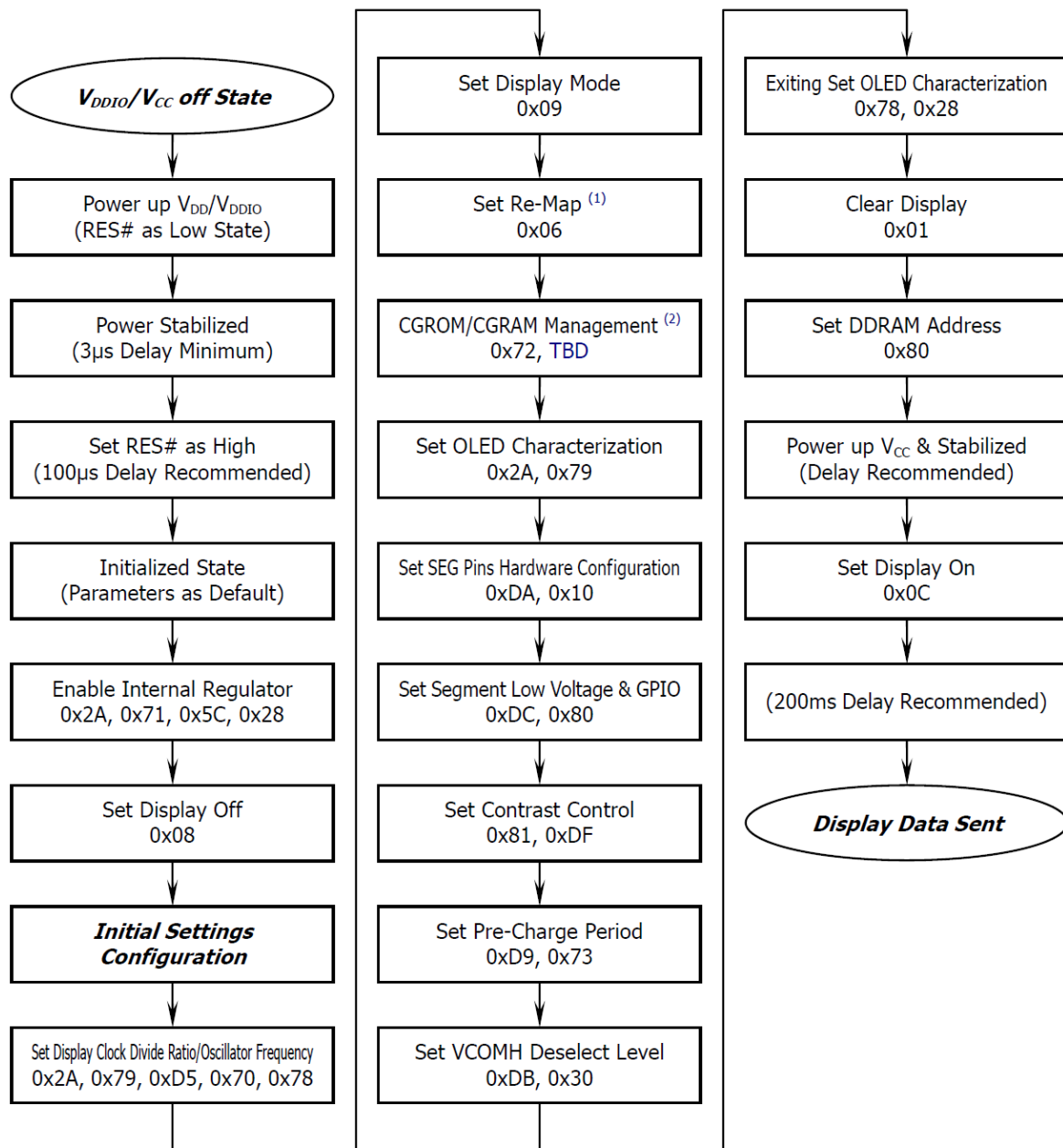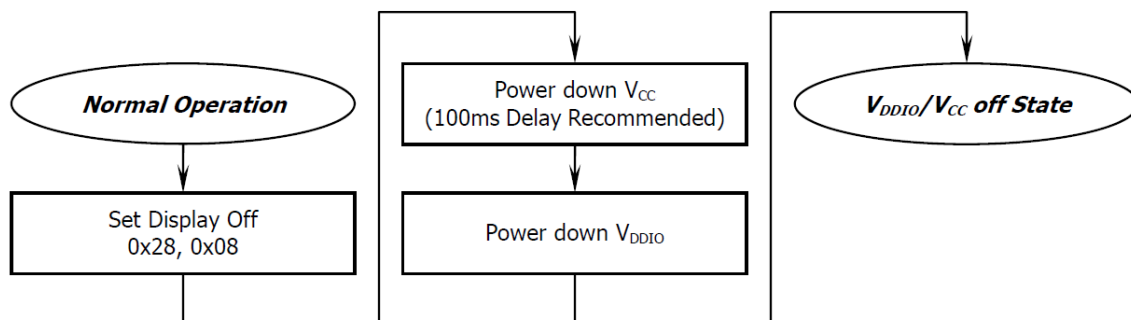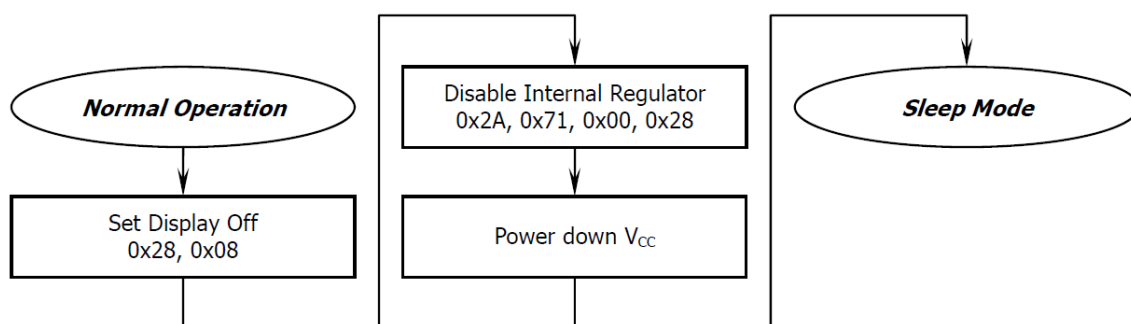| Product No.	DD-4C20WE-1A	REV. B		Page	22 / 41

\<Power down Sequence\>

```
┌─────────────────┐        ┌──────────────────────────┐        ┌──────────────────────────┐
│ Normal Operation│        │   Power down V_CC        │        │ V_DD/V_DDIO/V_CC off State│
└────────┬────────┘        │ (100ms Delay Recommended)│        └──────────────────────────┘
         │                 └────────────┬─────────────┘
┌────────▼────────┐        ┌────────────▼─────────────┐
│ Set Display Off │        │  Power down V_DD/V_DDIO   │
│   0x28, 0x08    │        └──────────────────────────┘
└─────────────────┘
```

\<Entering Sleep Mode\>

```
┌─────────────────┐        ┌──────────────────────────┐
│ Normal Operation│        │   Power down V_CC        │
└────────┬────────┘        └────────────┬─────────────┘
         │                 ┌────────────▼─────────────┐
┌────────▼────────┐        │      Sleep Mode          │
│ Set Display Off │        └──────────────────────────┘
│   0x28, 0x08    │
└─────────────────┘
```

\<Exiting Sleep Mode\>

```
┌─────────────────┐        ┌──────────────────────────┐        ┌──────────────────────────┐
│   Sleep Mode    │        │    Set Display On        │        │   Normal Operation        │
└────────┬────────┘        │     0x28, 0x0C           │        └──────────────────────────┘
         │                 └────────────┬─────────────┘
┌────────▼────────┐        ┌────────────▼─────────────┐
│ Power up V_CC & │        │ (200ms Delay Recommended) │
│   Stabilized    │        └──────────────────────────┘
│(Delay Recommend)│
└─────────────────┘
```

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5.4.2 5V I/O Application

```
┌─────────────────────┐     ┌─────────────────────┐     ┌─────────────────────────────┐
│  V_DDIO/V_CC off     │     │  Set Display Mode   │     │ Exiting Set OLED            │
│  State               │     │  0x09               │     │ Characterization 0x78, 0x28 │
└─────────────────────┘     └─────────────────────┘     └─────────────────────────────┘
           │                           │                             │
┌─────────────────────┐     ┌─────────────────────┐     ┌─────────────────────┐
│ Power up V_DD/V_DDIO │     │ Set Re-Map (1)      │     │ Clear Display       │
│ (RES# as Low State)  │     │ 0x06                │     │ 0x01                │
└─────────────────────┘     └─────────────────────┘     └─────────────────────┘
           │                           │                             │
┌─────────────────────┐     ┌─────────────────────┐     ┌─────────────────────┐
│ Power Stabilized     │     │ CGROM/CGRAM         │     │ Set DDRAM Address    │
│ (3µs Delay Minimum)  │     │ Management (2)       │     │ 0x80                 │
└─────────────────────┘     │ 0x72, TBD           │     └─────────────────────┘
           │                 └─────────────────────┘                 │
┌─────────────────────┐                │                 ┌─────────────────────┐
│ Set RES# as High     │     ┌─────────────────────┐     │ Power up V_CC &      │
│ (100µs Delay         │     │ Set OLED            │     │ Stabilized           │
│ Recommended)         │     │ Characterization    │     │ (Delay Recommended)  │
└─────────────────────┘     │ 0x2A, 0x79          │     └─────────────────────┘
           │                 └─────────────────────┘                 │
┌─────────────────────┐                │                 ┌─────────────────────┐
│ Initialized State    │     ┌─────────────────────┐     │ Set Display On       │
│ (Parameters as       │     │ Set SEG Pins        │     │ 0x0C                 │
│ Default)             │     │ Hardware Config     │     └─────────────────────┘
└─────────────────────┘     │ 0xDA, 0x10          │                 │
           │                 └─────────────────────┘     ┌─────────────────────┐
┌─────────────────────┐                │                 │ (200ms Delay         │
│ Enable Internal      │     ┌─────────────────────┐     │ Recommended)         │
│ Regulator            │     │ Set Segment Low     │     └─────────────────────┘
│ 0x2A, 0x71, 0x5C,    │     │ Voltage & GPIO      │                 │
│ 0x28                 │     │ 0xDC, 0x80          │     ┌─────────────────────┐
└─────────────────────┘     └─────────────────────┘     │ Display Data Sent    │
           │                           │                 └─────────────────────┘
┌─────────────────────┐     ┌─────────────────────┐
│ Set Display Off      │     │ Set Contrast        │
│ 0x08                 │     │ Control             │
└─────────────────────┘     │ 0x81, 0xDF          │
           │                 └─────────────────────┘
┌─────────────────────┐                │
│ Initial Settings     │     ┌─────────────────────┐
│ Configuration        │     │ Set Pre-Charge      │
└─────────────────────┘     │ Period 0xD9, 0x73   │
           │                 └─────────────────────┘
┌─────────────────────┐                │
│ Set Display Clock    │     ┌─────────────────────┐
│ Divide Ratio/Osc Freq│     │ Set VCOMH Deselect  │
│ 0x2A, 0x79, 0xD5,    │     │ Level 0xDB, 0x30    │
│ 0x70, 0x78           │     └─────────────────────┘
└─────────────────────┘
```

(1) This command could be programmable or defined by pin configuration.
(2) This command could be programmable or defined by pin configuration. The written value of the parameter should depend on the selection from section 5.5 and 5.6

If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

<Power down Sequence>

```
┌─────────────────────┐      ┌──────────────────────────────┐      ┌─────────────────────────┐
│  Normal Operation   │      │  Power down V_CC             │      │  V_DDIO/V_CC off State  │
│                     │      │  (100ms Delay Recommended)   │      │                         │
└─────────────────────┘      └──────────────────────────────┘      └─────────────────────────┘
           │                            │
           ▼                            ▼
┌─────────────────────┐      ┌──────────────────────────────┐
│  Set Display Off    │      │  Power down V_DDIO           │
│  0x28, 0x08         │      │                              │
└─────────────────────┘      └──────────────────────────────┘
```

Normal Operation → Set Display Off 0x28, 0x08 → Power down V_{CC} (100ms Delay Recommended) → Power down V_{DDIO} → V_{DDIO}/V_{CC} off State

<Entering Sleep Mode>

Normal Operation → Set Display Off 0x28, 0x08 → Disable Internal Regulator 0x2A, 0x71, 0x00, 0x28 → Power down V_{CC} → Sleep Mode

<Exiting Sleep Mode>

Sleep Mode → Enable Internal Regulator 0x2A, 0x71, 0x5C, 0x28 → Power up V_{CC} & Stabilized (Delay Recommended) → Set Display On 0x28, 0x0C → (200ms Delay Recommended) → Normal Operation

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5.5 BUILD-IN CGROM (CHARACTER GENERATOR ROM)

5.5.1 ROMA

ROM A (ROM[1:0] = [0:0])

Language: English, Irish, Spanish, Dutch (2), Danish, Norwegian, Swedish, Finnish, Czech (7), Slovene, Hungarian (2), Turkish (1)

The number in the parentheses is showing how many letters might be needed to build and define additionally at CGRAM. The darker background is showing the maximum addresses (00h~07h) those could be allocated by OPR[1:0] setting.

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5.5.2 ROMB

ROM B (ROM[1:0] = [0:1])

Language: English, Irish, Portuguese, Spanish, French (1), Italian, German, Dutch (2), Icelandic, Danish, Norwegian, Swedish, Polish (8), Czech (8), Hungarian (2), Romanian (5), Turkish, Vietnamese (6), Russian (Small Letters)
The number in the parentheses is showing how many letters might be needed to build and define additionally at CGRAM. The darker background is showing the maximum addresses (00h~07h) those could be allocated by OPR[1:0] setting.

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5.5.3 ROMC

ROM C (ROM[1:0] = [1:0])

Language: English, Dutch (2), Japanese, Greek (Small Letters)

The number in the parentheses is showing how many letters might be needed to build and define additionally at CGRAM. The darker background is showing the maximum addresses (00h~07h) those could be allocated by OPR[1:0] setting.

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5.6 SELF-DEFINED CGRAM (CHARACTER GENERATOR RAM)

8 Addresses Available for Self-Defined Characters (OPR[1:0] = [0:0])

8 Addresses Available for Self-Defined Characters (OPR[1:0] = [0:1])

6 Addresses Available for Self-Defined Characters (OPR[1:0] = [1:0])

0 Address Available for Self-Defined Characters (OPR[1:0] = [1:1])

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6 PACKAGING AND LABELLING SPECIFICATION
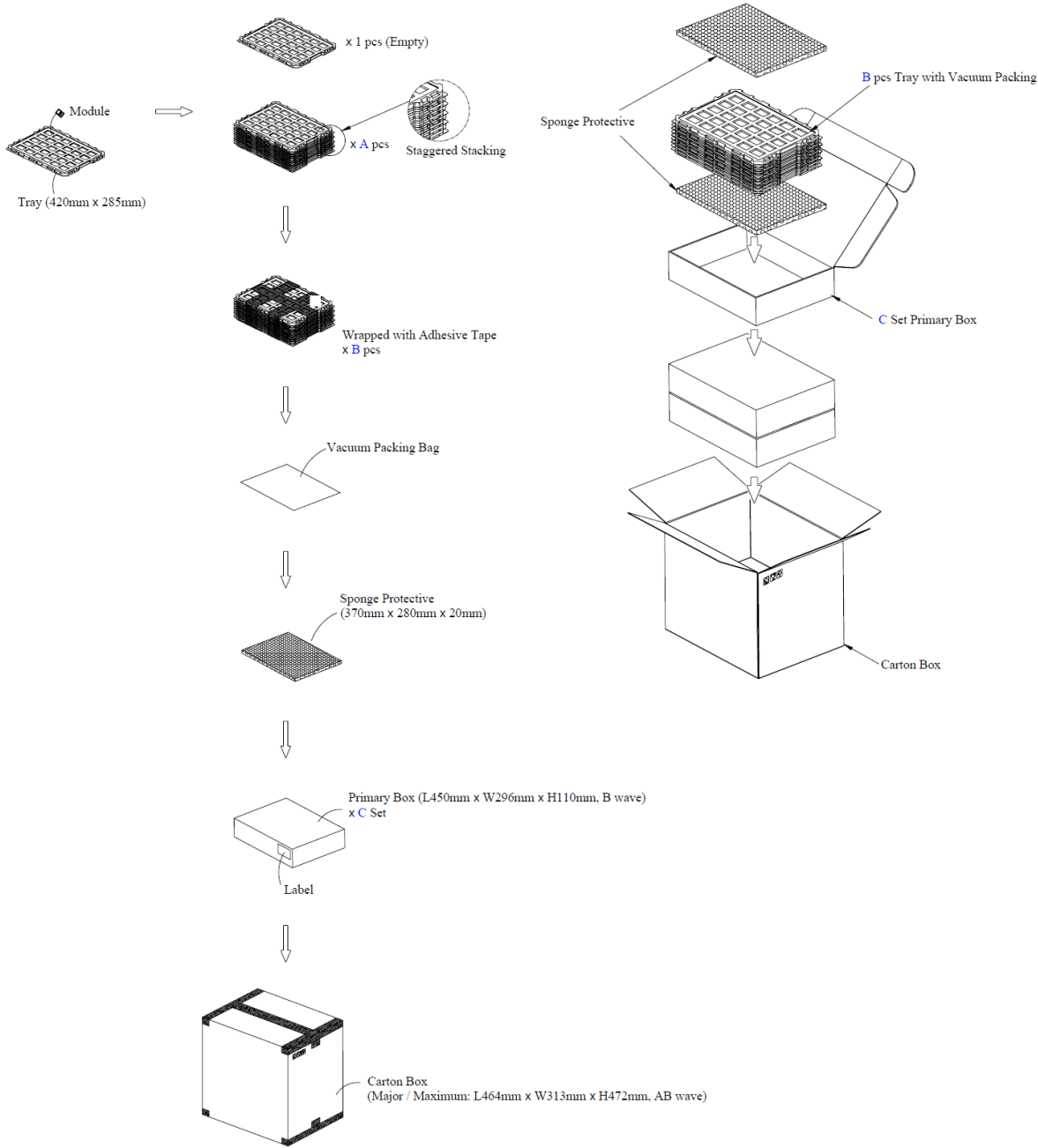
Item	Quantity
Module	320 per Primary Box
Holding Trays (A)	20 per Primary Box
Total Trays (B)	21 per Primary Box (Including 1 Empty Tray)
Primary Box (C)	1~4 per Carton (4 as Major / Maximum)

7 QUALITY ASSURANCE SPECIFICATION

7.1 CONFORMITY

The performance, function and reliability of the shipped products conform to the Product Specification.

7.2 DELIVERY ASSURANCE

7.2.1 DELIVERY INSPECTION STANDARDS

IPC-AA610, class 2 electronic assemblies standard

7.2.2 Zone definition

A   Active

B   Outside Active
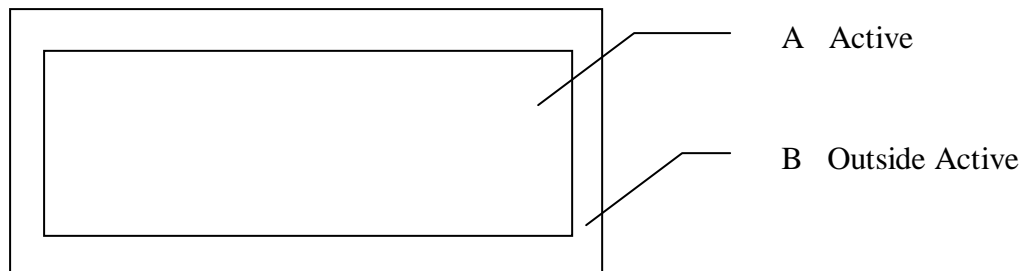
7.2.3 Visual inspection

Test and measurement to be conducted under following conditions :
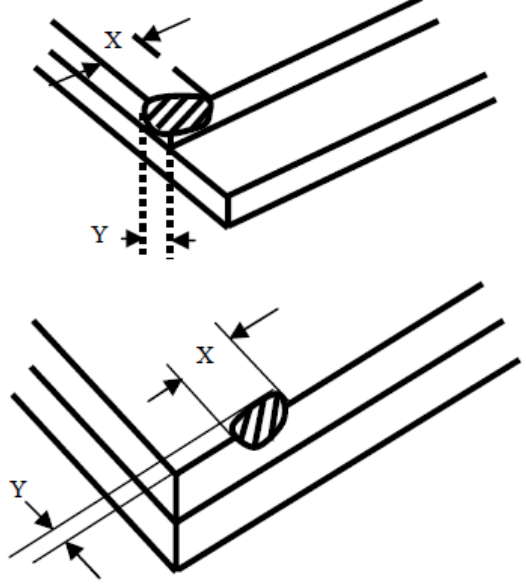
Temperature:	23±5℃
Humidity:	55±15%RH
Fluorescent lamp:	30 W
Distance between the Panel & Eyes of the Inspector:	≧30cm
Distance between the Panel & the lamp:	≧50cm

Finger glove (or finger cover) must be worn by the inspector.
Inspection table or jig must be anti-electrostatic
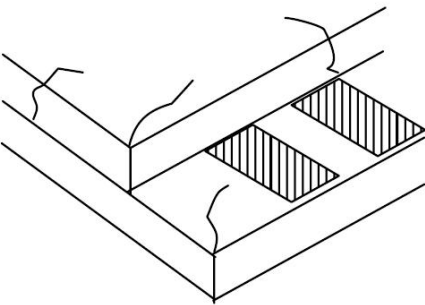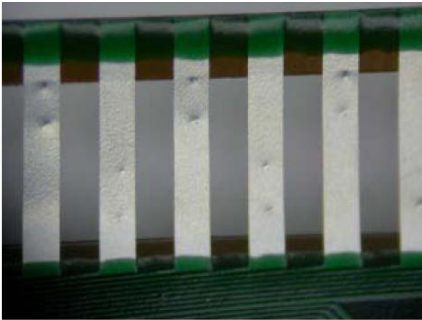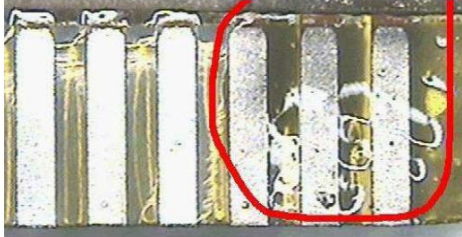
7.2.4 Standard of appearance inspection

Partition	AQL	Definition
Major	0.65	Defects in Pattern Check (Display On)
Minor	1.0	Defects in Cosmetic Check (Display Off)

Check Item	Classification	Criteria
Panel General Chipping	Minor	X > 6 mm (Along with Edge) Y > 1 mm (Perpendicular to edge)
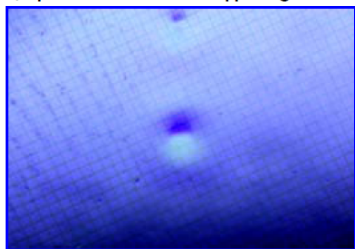
Check Item	Classification	Criteria
Panel Crack	Minor	Any crack is not allowable.
Copper Exposed (Even Pin or Film)	Minor	Not Allowable by Naked Eye Inspection
Film or Trace Damage	Minor	
Terminal Lead Prober Mark	Acceptable	
Glue or Contamination on Pin (Couldn't Be Removed by Alcohol)	Minor	
Ink Marking on Back Side of panel (Exclude on Film)	Acceptable	Ignore for Any

Check Item	Classification	Criteria
Any Dirt & Scratch on Polarizer's Protective Film	Acceptable	Ignore for not Affect the Polarizer

Scratches, Fiber, Line-Shape Defect (On Polarizer)	Minor	$W \le 0.1$ Ignore
		$W > 0.1$
		   $L \le 2$ $n \le 1$
		   $L > 2$ $n = 0$

Dirt, Black Spot, Foreign Material, (On Polarizer)	Minor	$\Phi \le 0.1$ Ignore $0.1 < \Phi \le 0.25$ $n \le 1$ $0.25 < \Phi$ $n = 0$
Dent, Bubbles, White spot (Any Transparent Spot on Polarizer)	Minor	$\Phi \le 0.5$ ➔ Ignore if no Influence on Display $0.5 < \Phi$ $n = 0$
Fingerprint, Flow Mark (On Polarizer)	Minor	Not Allowable
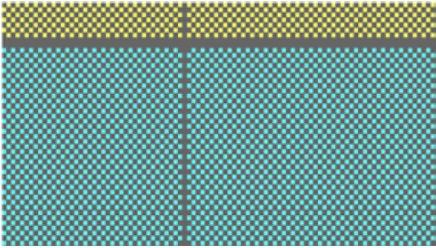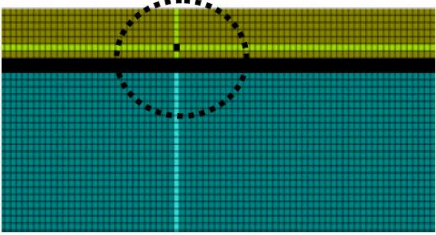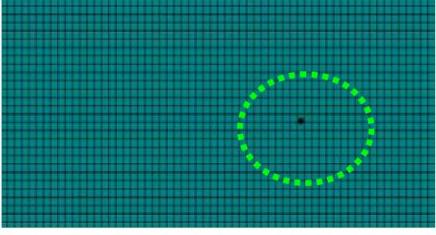
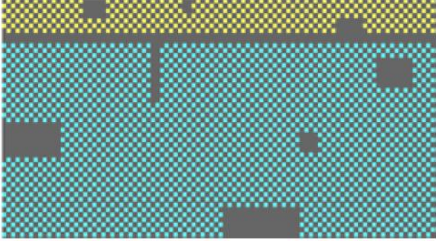*   Protective film should not be tear off when cosmetic check.

** Definition of W & L & Φ (Unit: mm): $\Phi = (a + b) / 2$

L

W

b: Minor Axis

a: Major Axis
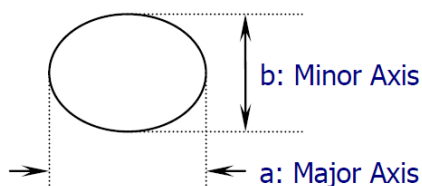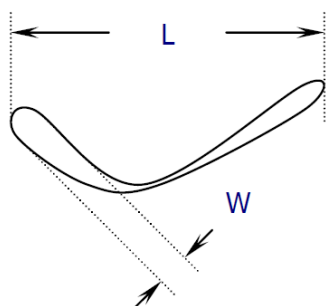
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Check Item	Classification	Criteria
No Display	Major	
Missing Line	Major	
Pixel Short	Major	
Darker Pixel	Major	
Wrong Display	Major	
Un-uniform	Major	

7.3 DEALING WITH CUSTOMER COMPLAINTS

7.3.1 Non-conforming analysis

Purchaser should supply Densitron with detailed data of non-conforming sample.
After accepting it, Densitron should complete the analysis in two weeks from receiving the sample.
If the analysis cannot be completed on time, Densitron must inform the purchaser.

7.3.2 Handling of non-conforming displays

If any non-conforming displays are found during customer acceptance inspection which Densitron is clearly responsible for, return them to Densitron.
Both Densitron and customer should analyse the reason and discuss the handling of non-conforming displays when the reason is not clear.
Equally, both sides should discuss and come to agreement for issues pertaining to modification of Densitron quality assurance standard.

8 RELIABILITY SPECIFICATION

8.1 RELIABILITY TESTS

Test Item	Test Condition	Criteria
High Temperature Operation	85°C, 240 hours	The operational functions work.
Low Temperature Operation	-40°C, 240 hours	
High Temperature Storage	90°C, 240 hours	
Low Temperature Storage	-40°C, 240 hours	
High Temperature & High Humidity Storage	60°C, 90%RH, 240hours	
Thermal Shock	-40°C ⇔ 85°C, 100 cycles. 60 Mins dwell	

- The samples used for above tests do not include polarizer.
- No moisture condensation is observed during tests.

8.1.1 FAILURE CHECK STANDARD

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure teat at 23±5 °C; 55±15% RH

8.2 LIFE TIME

| Item	Description
1	Function, performance, appearance, etc. shall be free from remarkable deterioration more than 30,000 hours under 80 cd/m² brightness and 50% Checkerboard, humidity (50% RH), and in area not exposed to direct sunlight. Vcc=12.0V, Ta=25°C, 50% Checkerboard. Software configuration follows Section 5.4 Initialization.
2	End of lifetime is specified as 50% of initial brightness. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

9 HANDLING PRECAUTIONS

9.1 HANDLING PRECAUTIONS

1) Since the display panel is being made of glass, do not apply mechanical impacts such us dropping from a high position.
2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.
3) If pressure is applied to the display surface or its neighborhood of the OEL display module, the cell structure may be damaged and be careful not to apply pressure to these sections.
4) The polarizer covering the surface of the OEL display module is soft and easily scratched. Please be careful when handling the OEL display module.
5) When the surface of the polarizer of the OEL display module has soil, clean the surface. It takes advantage of by using following adhesion tape.
   * Scotch Mending Tape No. 810 or an equivalent
   Never try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy.
   Also, pay attention that the following liquid and solvent may spoil the polarizer:
   * Water
   * Ketone
   * Aromatic Solvents
6) Hold OEL display module very carefully when placing OEL display module into the system housing. Do not apply excessive stress or pressure to OEL display module. And, do not over bend the film with electrode pattern layouts. These stresses will influence the display performance. Also, secure sufficient rigidity for the outer cases.
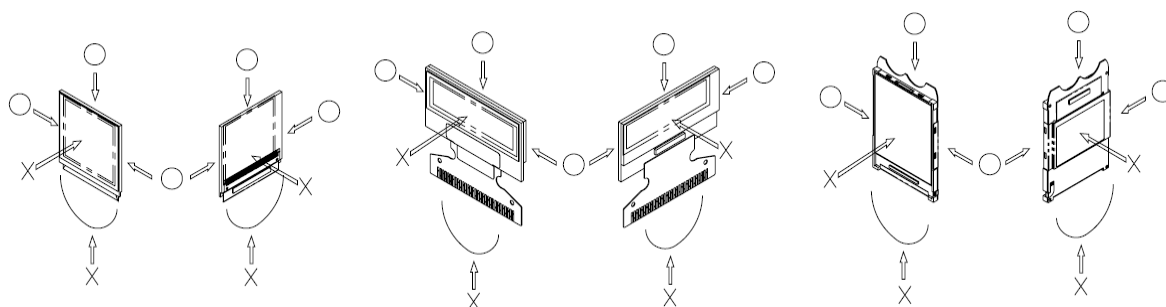
7) Do not apply stress to the LSI chips and the surrounding molded sections.
8) Do not disassemble nor modify the OEL display module.
9) Do not apply input signals while the logic power is off.
10) Pay sufficient attention to the working environments when handing OEL display modules to prevent occurrence of element breakage accidents by static electricity.
    * Be sure to make human body grounding when handling OEL display modules.
    * Be sure to ground tools to use or assembly such as soldering irons.
    * To suppress generation of static electricity, avoid carrying out assembly work under dry environments.

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* Protective film is being applied to the surface of the display panel of the OEL display module. Be careful since static electricity may be generated when exfoliating the protective film.

11) Protection film is being applied to the surface of the display panel and removes the protection film before assembling it. At this time, if the OEL display module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).

12) If electric current is applied when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

9.2 STORAGE PRECAUTIONS

1) When storing OEL display modules, put them in static electricity preventive bags avoiding exposure to direct sun light nor to lights of fluorescent lamps, etc. and, also, avoiding high temperature and high humidity environments or low temperature (less than 0°C) environments. (We recommend you to store these modules in the packaged state when they were shipped from Densitron Technologies Plc.) At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.

2) If electric current is applied when water drops are adhering to the surface of the OEL display module, when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

9.3 DESIGNING PRECAUTIONS

1) The absolute maximum ratings are the ratings which cannot be exceeded for OEL display module, and if these values are exceeded, panel damage may be happen.

2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the VIL and VIH specifications and, at the same time, to make the signal line cable as short as possible.

3) We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (V_{DD}). (Recommend value: 0.5A)

4) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighboring devices.

5) As for EMI, take necessary measures on the equipment side basically.

6) When fastening the OEL display module, fasten the external plastic housing section.

7) If power supply to the OEL display module is forcibly shut down by such errors as taking out the main battery while the OEL display panel is in operation, we cannot guarantee the quality of this OEL display module.

8) The electric potential to be connected to the rear face of the IC chip should be as follows: US2066
   * Connection (contact) to any other potential than the above may lead to rupture of the IC.

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9.4 OTHER PRECAUTIONS

1) When an OEL display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur. Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored. Also, there will be no problem in the reliability of the module.

2) To protect OEL display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the OEL display modules.
   * Pins and electrodes
   * Pattern layouts such as the FPC

3) With this OEL display module, the OEL driver is being exposed. Generally speaking, semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if this OEL driver is exposed to light, malfunctioning may occur.
   * Design the product and installation method so that the OEL driver may be shielded from light in actual usage.
   * Design the product and installation method so that the OEL driver may be shielded from light during the inspection processes.

4) Although this OEL display module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed. It therefore is necessary to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.

5) We recommend you to construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.

10 SUPPORTED ACCESSORIES

10.1 DUO KIT

Densitron has developed an easy to use yet powerful development and demonstration tool for driving its range of Passive Matrix OLED displays from the USB port of a PC.
DUO (Densitron USB OLED) kit is hot pluggable and does not require extra cables or power supply to run, allowing users to be up and running in minutes.

The kit consists of an OLED display with transition Board, USB controller card, mini USB cable and a CD with software application and drivers.

Part number: UNDER DEVELOPMENT

10.1 TRANSITION BOARD CARD

A Transition board card is like a daughterboard which is meant to be a circuit board for connections between the baseboards (DUO).
It has connector pins for interfacing between the display and the baseboards.
It also includes the OLED display.
Part number: UNDER DEVELOPMENT

10.2 CONNECTOR BOARD CARD

A Connector board card is also a daughterboard which is a circuit board for connection between a microprocessor or microcontroller (customer's system).
Part number: UNDER DEVELOPMENT

10.3 CONNECTOR

Type: hot bar soldering process
No. of connections: 33
Pitch: 0.70mm

10.4 APPLICATION NOTES AND EXAMPLE CODES

On request to Densitron

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