OLED DISPLAY MODULE

Product Specification

CUSTOMER	**STANDARD**	
PRODUCT NUMBER	**DD-9664FC-2A**	
CUSTOMER APPROVAL		

INTERNAL APPROVALS		
Product Mgr	Doc Control	Electr. Eng
Bruno Recaldini	**Anthony Perkins**	**Bazile Peter**
Date: 01/02/07	Date: 01/02/07	Date: 01/02/07

Rev.	Date	Page	Chapt.	Comment	ECR no.
A	Feb 2007			Production Release	
B	28 Nov 12	30	10	Add chapter 10 supported accessories	

1 MAIN FEATURES

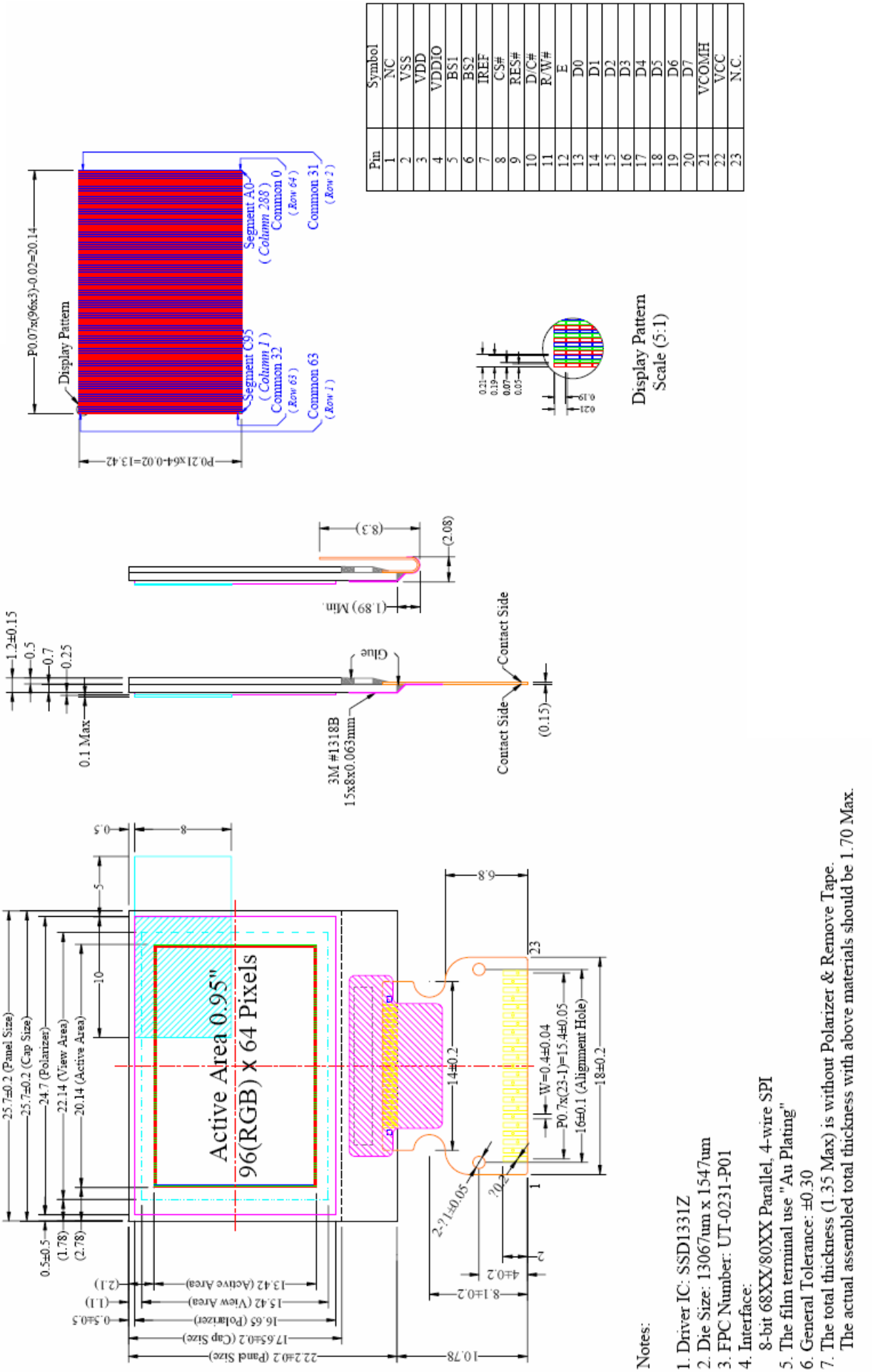
ITEM	CONTENTS
Display Format	96 (R.G.B.) x 64 Dots
Overall Dimensions(W*H*T)	Glass 25.70 x 22.20 x 1.5 mm
Active Area(W*H)	20.14 x 13.42 mm
Viewing Area(W*H)	22.14 x 15.42 mm
Display Mode	Passive Matrix (0.95")
Display Colour	65,536 Colour
Driving Method	1 / 64 duty
Driver IC	SSD1331
Operating temperature	-30℃ ~ +70℃
Storage temperature	-40℃ ~ +80℃

2 MECHANICAL SPECIFICATION

2.1 MECHANICAL CHARACTERISTICS

ITEM	CHARACTERISTIC	UNIT
Display Format	96 (RGB x 64	Dots
Overall Dimensions	25.70 x 22.20 x 1.50	mm
Active Area(W*H)	20.14 x 13.42	mm
Viewing Area(W*H)	22.14 x 15.42	mm
Dot Size	0. 05 x (RGB) x 0.19	mm
Dot Pitch	0.07 x (RGB) x 0.21	mm
Weight	1.8	g
IC Controller/Driver	SSD1331	

2.2 MECHANICAL DRAWING



3 ELECTRICAL SPECIFICATION

3.1 ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min	Max	Unit	Note
Supply Voltage	V_{DD}	-0.3	4	V	Note 1,2
Driver Supply Voltage	Vcc	0	15	V	
V_{CC} Supply Current	I_{CC}	-	25	mA	
Operating Temperature	Top	-30	70	°C	-
Storage Temperature	Tst	-40	80	°C	-
Static Electricity	Be sure that you are grounded when handling displays.				

Note 1: All the above voltages are on the basis of "GND=0V".
Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it's desirable to use this module under the conditions according to Section 3 "Electrical Characteristics".

3.2 ELECTRICAL CHARACTERISTICS

3.2.1 DC CHARACTERISTICS

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Logic	V_{DD}		2.4	2.8	3.5	V
Supply Voltage for I/O pins	V_{DDIO}		1.6	2.8	3.5	V
Driver Supply Voltage	V_{CC}		-	14.0	-	V
Operating Current for V_{DD}	I_{DD}	Note 1	-	0.2	0.6	mA
		Note 2	-	0.2	0.6	mA
Operating Current for V_{CC}	I_{CC}	Note 1	-	8	11	mA
		Note 2	-	13.5	18	mA
Sleep Mode Current for VDD	I_{DD} sleep		-	1	2	µA
Sleep Mode Current for VCC	I_{CC} sleep		-	<2	2	µA
High Level Input	V_{IH}	I out = 100µA, 3.3MHz	$0.8xV_{DD}$	-	V_{DDIO}	V
Low Level Input	V_{IL}		0	-	$0.2xV_{DDIO}$	V
High Level Output	V_{OH}		$0.9xV_{DDIO}$	-	V_{DDIO}	V
Low Level Output	V_{OL}		0	-	$0.1xV_{DDIO}$	V

Note 1: V_{DD} = 2.8V, V_{CC} = 14V, Software Initial Setting follow Section. 6 “Software initial setting”, 50% Display area turn on.

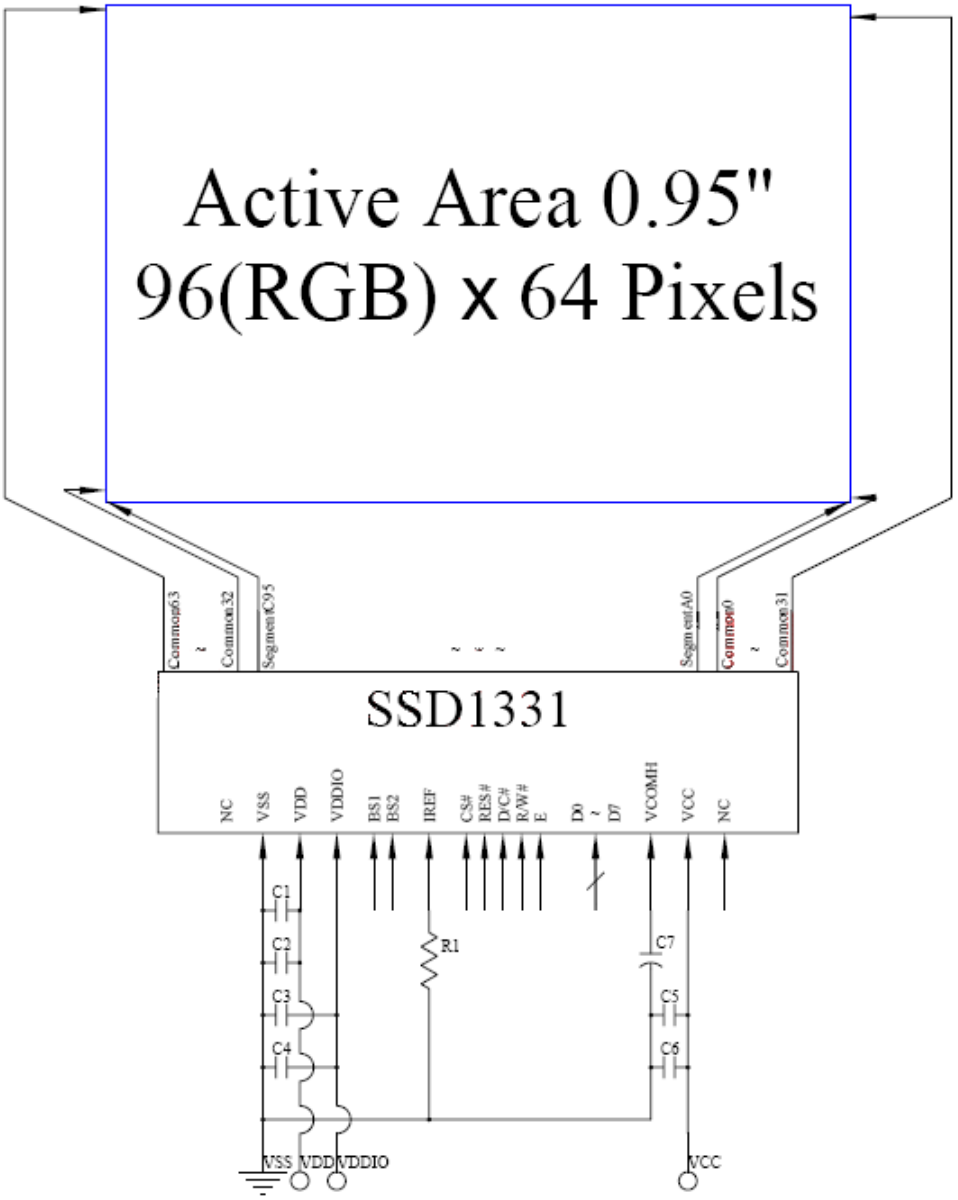
Note 2: V_{DD} = 2.8V, V_{CC} = 14V, Software Initial Setting follow Section. 6 “Software initial setting”, 100% Display area turn on.

3.3 INTERFACE PIN ASSIGNMENT

<table>
<tr><th>No.</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>1</td><td>N.C.</td><td>-</td><td>Reserved Pin (Supporting Pin).
The supporting pins can reduce the influences from stresses on the function pins.</td></tr>
<tr><td>2</td><td>VSS</td><td>P</td><td>Ground of System.
This is a ground pin. It also acts as a reference for the logic pins, the OLED driving voltages and the analog circuits. It must be connected to external ground.</td></tr>
<tr><td>3</td><td>VDD</td><td>P</td><td>Power Supply for Interface Logic Level.
This is a voltage supply pin. It must be connected to external source.</td></tr>
<tr><td>4.</td><td>VDDIO</td><td>P</td><td>Power Supply for Interface Logic Level.
It Should match with the MCU interface voltage level. VDDIO must always be equal or lower than VDD</td></tr>
<tr><td>5</td><td>BS1</td><td rowspan="2">I</td><td rowspan="2">Communicating Protocol Select.
These pins are MCU interface selection input. See the following table:
<table>
<tr><th></th><th>68XX-parallel</th><th>80XX-parallel</th><th>Serial</th></tr>
<tr><td>BS1</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>BS2</td><td>1</td><td>1</td><td>0</td></tr>
</table></td></tr>
<tr><td>6</td><td>BS2</td></tr>
<tr><td>7</td><td>IREF</td><td>I</td><td>Current Reference for Brightness Adjustment.
This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current at 10uA.</td></tr>
<tr><td>8</td><td>CS#</td><td>I</td><td>Chip Select.
This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.</td></tr>
<tr><td>9</td><td>RES#</td><td>I</td><td>Power Reset for Controller and Driver.
This pin is reset signal input. When the pin is low, initialization of the chip executed.</td></tr>
<tr><td>10</td><td>D/C#</td><td>I</td><td>Data/Command Control.
This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 is treated as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register. For detail relationship to MCU interface signal, please refer to the Timing Characteristics Diagrams.</td></tr>
<tr><td>11</td><td>R/W#(WR#)</td><td>I</td><td>Read/Write Select or Write.
This pin is MCU interface input. When interface to a 68XX-series microprocessor, this pin will be used as the Read/Write (R/W#) selection input. Pull this pin to “High” for read mode and pull it to “Low” for write mode.
When 80XX interface mode is selected this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low.</td></tr>
<tr><td>12</td><td>E(RD#)</td><td>I</td><td>Read/ Write Enable or Read.
This pin is MCU interface input. When interfacing to a 68XX-series microprocessor this pin will be used as the Enable (E) signal. Read/Write operation is initiated when this pin is pulled high and the CS# is pulled low.
When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low.</td></tr>
<tr><td>13~20</td><td>D0~D7</td><td>I/O</td><td>Host Data Input / Output Bus
These pins are 8 bit bi-directional data bus to be connected to</td></tr>
</table>

			the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK.
21	VCOMH	O	Voltage Output High Level for COM Signal. The COM signal deselected voltage level. A tantalum capacitor should be connected between this pin and VSS
22	VCC	P	Power Supply for OLED panel. This is the most positive voltage supply pin of the chip. It should be supplied externally.
23	N.C.	-	Reserved Pin (Supporting Pin). The supporting pins can reduce the influences from stresses on the function pins.

3.4 BLOCK DIAGRAM



MCU Interface Selection: BS1 and BS2
Pins connected to MCU interface：D7~D0, E/RD#, R/W#, CS#, D/C# and RES#

C1, C3, C5 : 10 μF
C2, C4, C6 : 0.1 μF
C7 4.7 μF/20V Tntalum CAP
R1 : 1.2M, R1 = (Voltage at IREF – VSS) / IREF

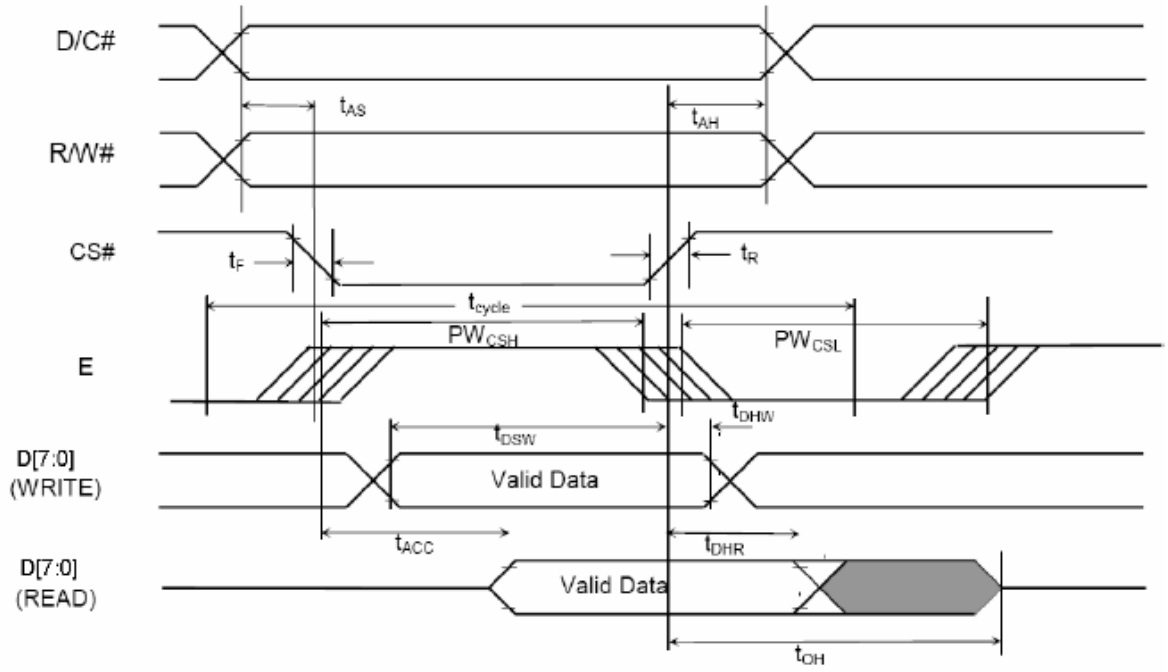
3.5 TIMING CHARACTERISTICS

3.5.1 AC CHARACTERISTICS

3.5.1.1 68XX-Series MPU Parallel Interface Timing Characteristics:

Characteristics	Symbol	Min	Max	Unit
Clock Cycle Time (write cycle)	t_{cycle}	130	-	ns
Control Pulse Low Width (write cycle)	PW_{CSL}	60	-	ns
Control Pulse High Width (write cycle)	PW_{CSH}	60	-	ns
Clock Cycle Time (read cycle)	t_{cycle}	200	-	ns
Control Pulse Low Width (read cycle)	PW_{CSL}	100	-	ns
Control Pulse High Width (read cycle)	PW_{CSH}	100	-	ns
Address Setup Time	tAS	0	-	ns
Address Hold Time	tAH	10	-	ns
Data Setup Time	tDSW	40	-	ns
Data Hold Time	tDHW	10	-	ns
Access Time	tACC	-	140	ns
Output Disable Time	tACC	-	70	ns
Rise Time	t_R	-	15	ns
Fall Time	t_F	-	15	ns

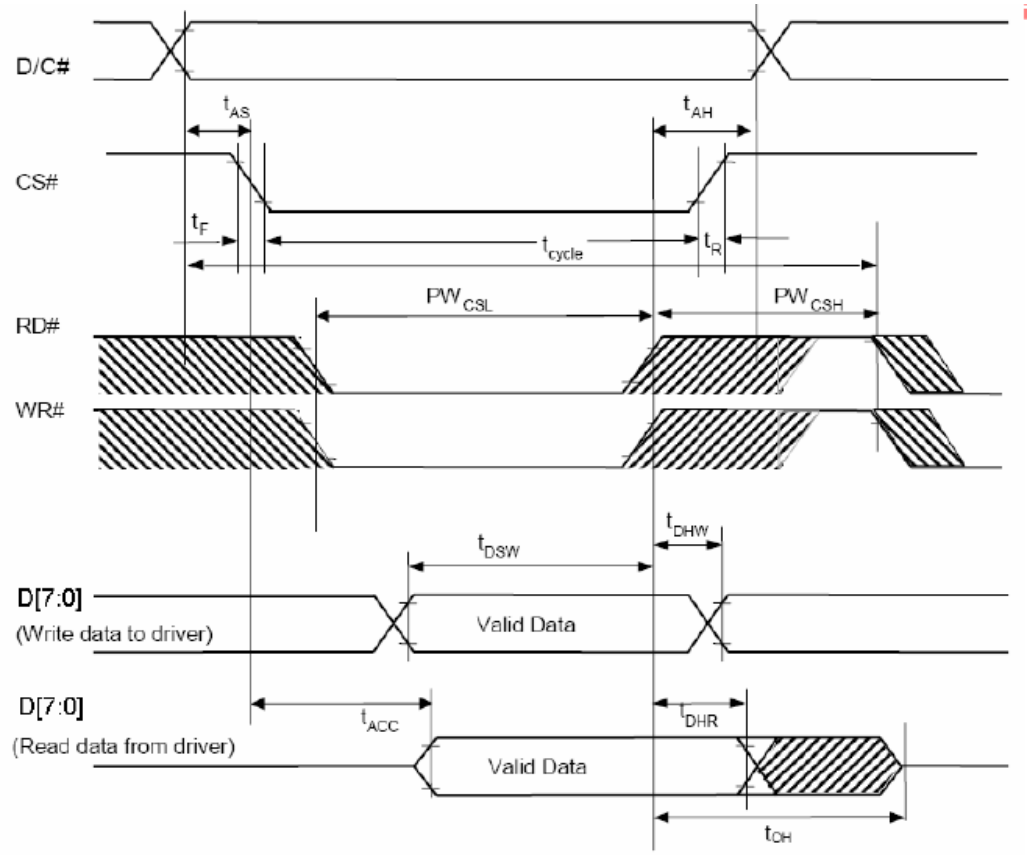
(V_{DD} – V_{SS} = 2.4V to 3.5V, V_{DDIO} =2.4V to V_{DD}, Ta = -40to +85˚C)



3.5.1.2 8080-Series MPU Parallel Interface Timing Characteristics:

Characteristics	Symbol	Min	Max	Unit
Clock Cycle Time	t_{cycle}	130	-	ns
Address Setup Time	t_{AS}	0	-	ns
Address Hold Time	t_{AH}	10	-	ns
Write Data Setup Time	t_{DSW}	40	-	ns
Write Data Hold Time	t_{DHW}	15	-	ns
Read Data Hold Time	t_{DHR}	20	-	ns
Output Disable Time	t_{OH}	-	70	ns
Access Time	t_{ACC}	-	140	ns
Chip Select Low Pulse Width (Read) Chip Select Low Pulse Width (Write)	PW_{CSL}	120 60	-	ns
Chip Select High Pulse Width (Read) Chip Select High Pulse Width (Write)	PW_{CSH}	60 60	-	ns
Rise Time	t_R	-	15	ns
Fall Time	t_F	-	15	ns

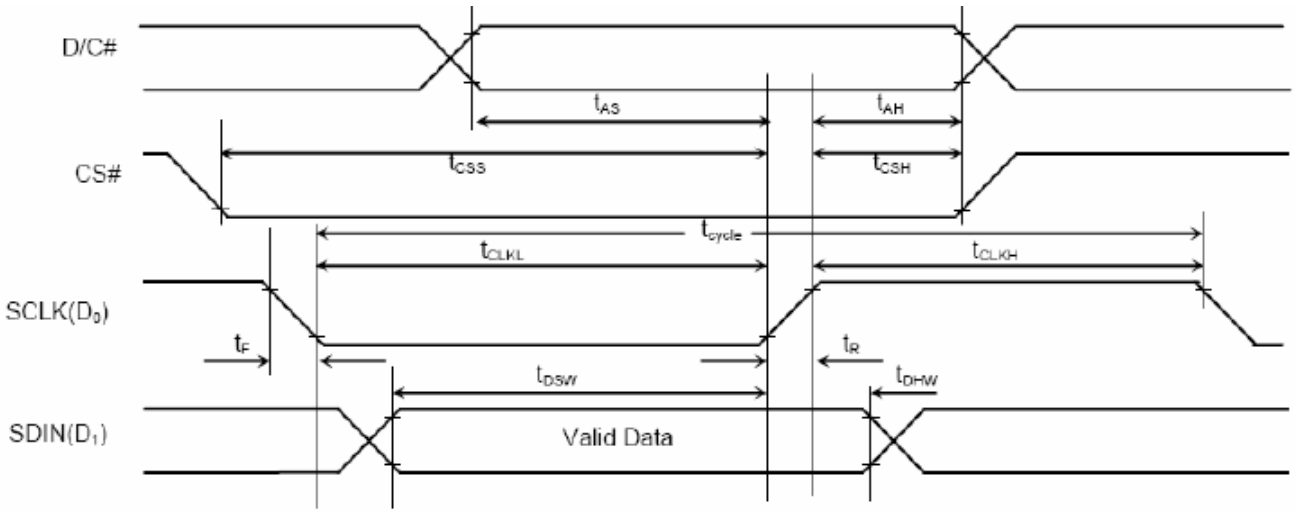
**** (V_{DD} – V_{SS} 2.4V to 3.5V, V_{DDIO} = 2.4V to V_{DD}, Ta = -40 to +85˚C)***

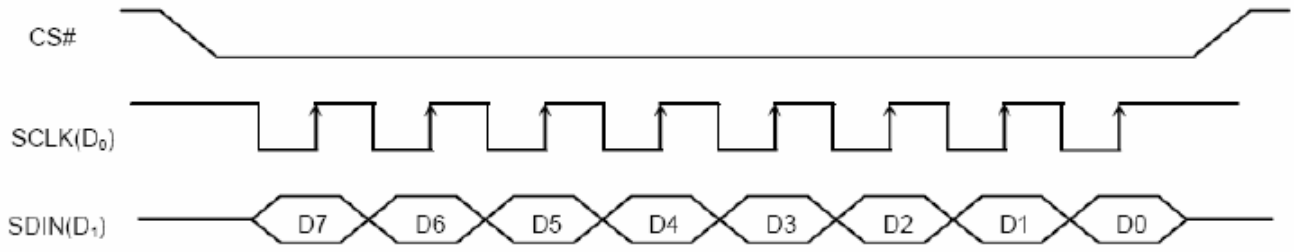


3.5.1.3 Serial Interface Timing Characteristics:

Characteristics	Symbol	Min	Max	Unit
Clock Cycle Time	t_{cycle}	150	-	ns
Address Setup Time	t_{AS}	40	-	ns
Address Hold Time	t_{AH}	40	-	ns
Chip Select Setup Time	t_{CSS}	75	-	ns
Chip Select Hold Time	t_{CSH}	60	-	ns
Write Data Setup Time	t_{DSW}	40	-	ns
Write Data Hold Time	t_{DHW}	40	-	ns
Clock Low Time	t_{CLKL}	75	-	ns
Clock High Time	t_{CLKH}	75		ns
Rise Time	t_R	-	15	ns
Fall Time	t_F	-	15	ns

**** (V_{DD} – V_{SS} = 2.4V to 3.5V, V_{DDIO} = 2.4V to V_{DD}, Ta = -40 to +85˚C)***





4 OPTICAL SPECIFICATION

4.1 OPTICAL CHARACTERISTICS

Characteristics	Symbol	Condition	Min	Typ	Max	Unit
Brightness(White)	L_{br}	With Polarizer Note 1	80	100	-	cd/m^2
C.I.E.(White)	(X)	With Polarizer	0.26	0.30	0.34	-
	(Y)		0.29	0.33	0.37	
C.I.E.(Red)	(X)	With Polarizer	0.60	0.64	0.68	-
	(Y)		0.30	0.34	0.38	
C.I.E.(Green)	(X)	With Polarizer	0.28	0.32	0.36	-
	(Y)		0.58	0.62	0.66	
C.I.E.(Blue)	(X)	With Polarizer	0.11	0.15	0.19	-
	(Y)		0.16	0.20	0.24	
Frame Rate			-	100	-	F/sec
Dark Room Contrast	CR	Shown as below	-	>1:1000	-	-
View Angle			>160	-	-	degree

Optical measurement taken at VDD = 2.8V, VCC = 14V and software configuration follows Section 6 “Software Initial Setting”

Note 1: Brightness (Lbr) and Driver Supply Voltage (V_{CC}) are subject to the change of the panel characteristics and the customer’s request.

5 APPLICATION NOTES

5.1 COMMANDS

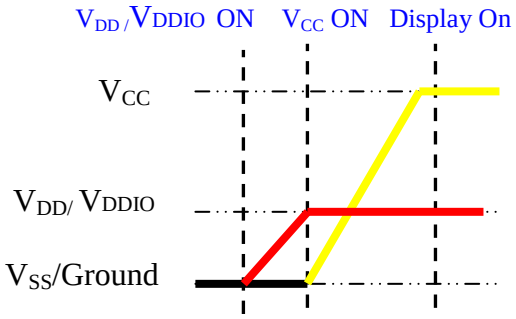
Please refer to the Technical Manual for the SSD1331.

5.2 POWER UP/DOWN SEQUENCE

To protect panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the panel enough time to complete the action of charge and discharge before/after the operation.

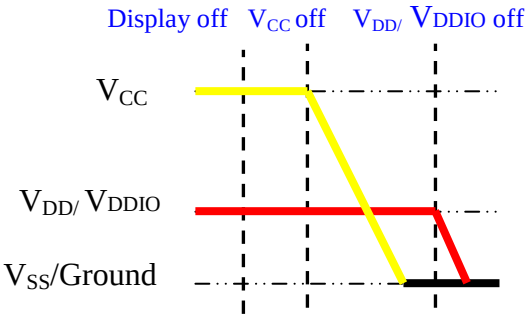
5.2.1 POWER UP SEQUENCE：

1. Power up V_{DD} & V_{DDIO}
2. Send Display off command
3. Clear Screen
4. Power up V_{CC}
5. Delay 100ms
   (When V_{DD}& V_{DDIO} is stable)
6. Send Display on command



5.2.2 POWER DOWN SEQUENCE：

1. Send Display off command
2. Power down V_{CC}
3. Delay 100ms
   (when V_{CC} is reach 0 and panel is completely discharges)
4. Power down V_{DD}& V_{DDIO}



5.3 RESET CIRCUIT

When RES# input is low, the chip is initialized with the following status:
1. Display is off
2. 64MUX Display Mode
3. Display start line is set at display RAM address 0
4. Display offset set to 0
5. Normal segment and display data column address and row address mapping (SEG0 mapped to address 00H and COM0 mapped to address 00H)
6. Column address counter is set at 0
7. Master contrast control register is set at 0FH
8. Individual contrast control registers of colour A, B and C are set at 80H.
9. Shift register data clear in serial interface
10.Normal display mode (Equivalent to A4 command)

5.4 APPLICATION EXAMPLE

Command usage and explanation of an actual example

< Initialization Setting >

Set Display On/Off (1010111X)
10101110=>0xAE (Display Off)

Set Display Mode (101001XX)
10100100=>0xA4 (Normal Display Mode)

Set Display Clock Divide Ratio / Oscillator Frequency
(10110011 with XXXXXXXX)

Set Display Offset
(10100010 with XXXXXXXX)

Set Multiplex Ratio
(11001000 with XXXXXXXX)

Set Master Configuration
(10101101 with 1000111X)
10001110=>0x8E (External VCC supply selected)

Set Display Start Line
(10100001 with XXXXXXXX)
Set Segment Re-map & Data Format
(10100000 with XXXXXXXX)

Set Master Current Control
(10000111 with ****XXXX)
Set Contrast Control for Colour “A”
(10000001 with XXXXXXXX)
Set Contrast Control for Colour “B”
(10000010 with XXXXXXXX)
Set Contrast Control for Colour “C”
(10000011 with XXXXXXXX)

Set Pre-charge Level
(10111011 with **XXXXXX)
Set Second Pre-charge speed of colour A
(10001010 with XXXXXXXX
Set Second Pre-charge speed of Colour B
(10001011 with XXXXXXXX)
Set Second Pre-charge speed of Colour C
(10001100 with XXXXXXXX)
Set VCOMH
(10111110 with 00XXXXX0)

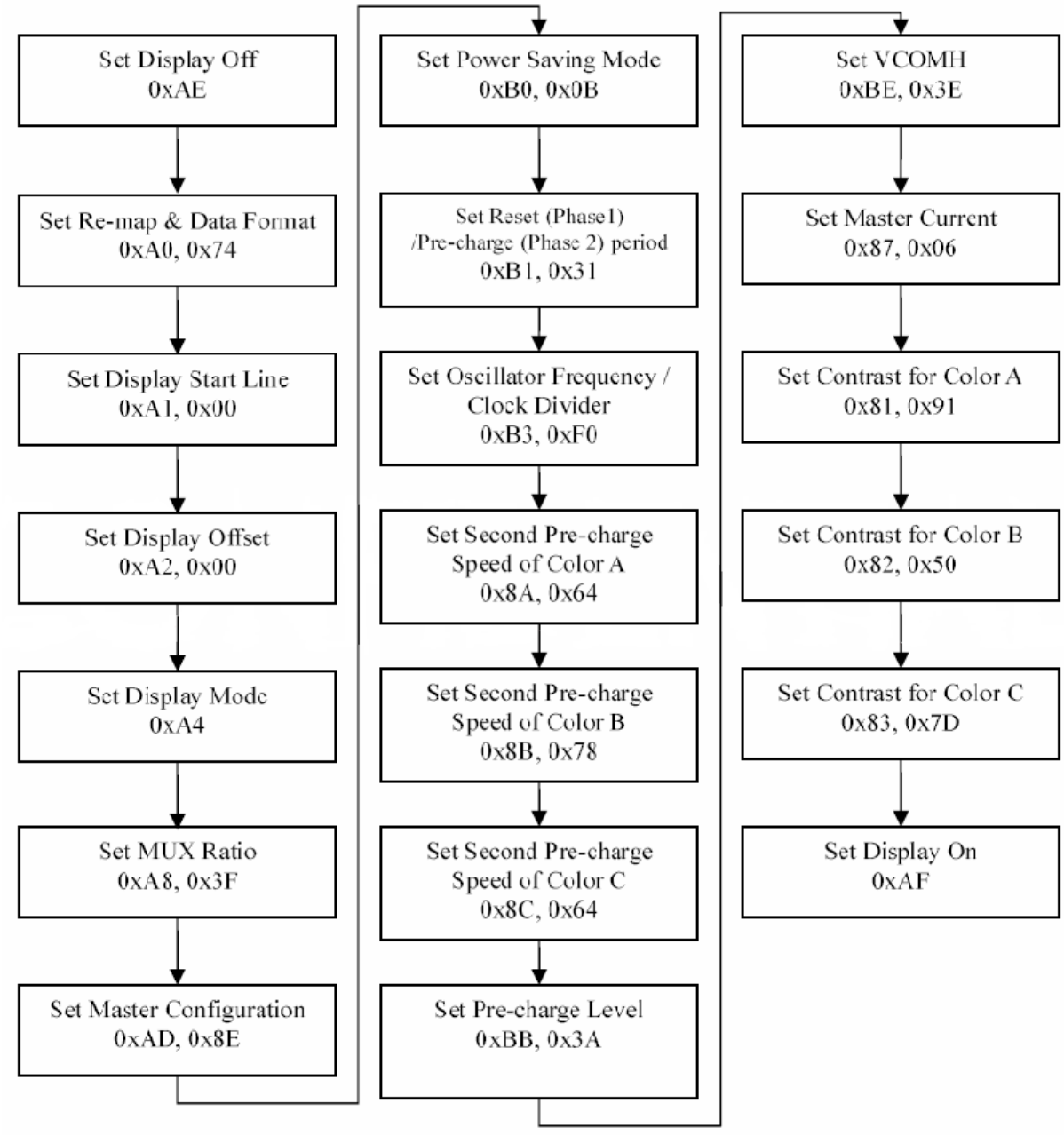
Set Phase 1 & 2 Period Adjustment
(10110001 with XXXXXXXX)
Set Power Saving Mode
(10110000 with 000XXXXX)

Set Display On/Off (1010111X)
10101111=> 0xAF (Display On)

<Display Boundary Settings>
Set Colum Address
(00010101 with XXXXXXXX for Start & XXXXXXXX for End)
Set Row Address
(01110101 with XXXXXXXX for Start & XXXXXXXX for End)

If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

6 SOFTWARE INITIAL SETTING



7 PACKAGING AND LABELLING SPECIFICATION

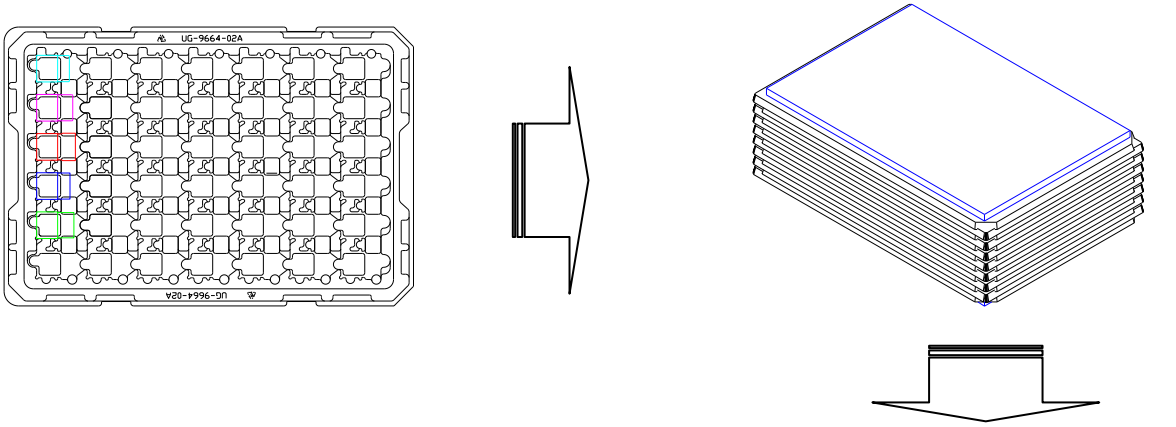
7.1 PACKAGING

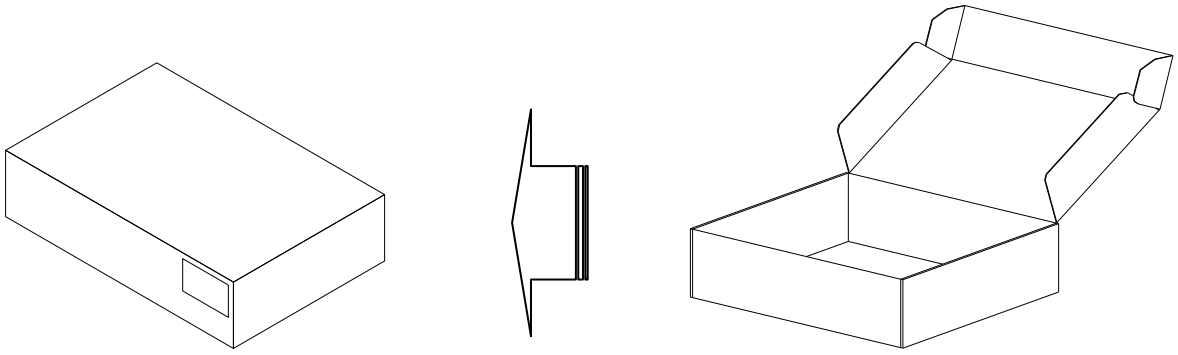
7.1.1 Material

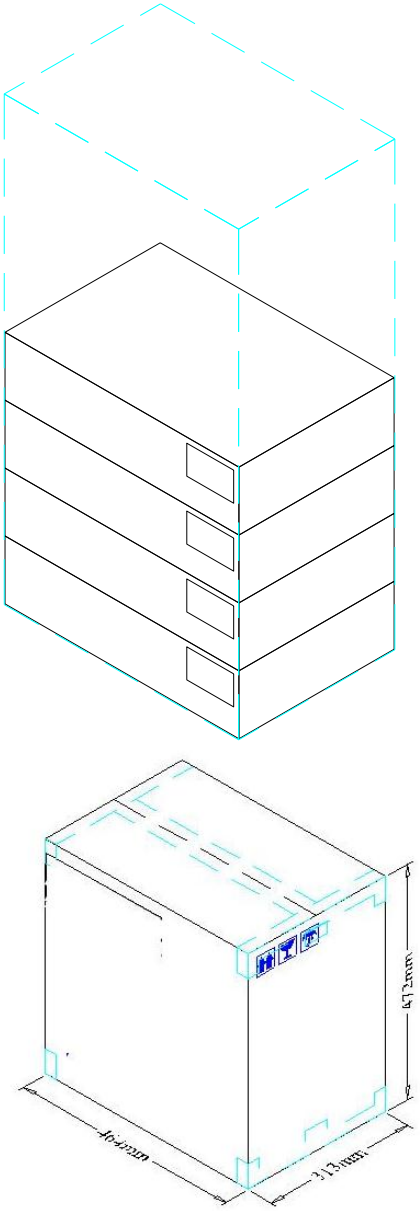
	Item	Part code	Dimensions (mm)	Unit weight (kg)	Quantity
1	Module	DD-9664FC-2A	25.7*22.1*1.5	0.002	2520
2	Tray	*****	***	0.010	
3	Inner box	*****	***	0.250	4
4	Carton	*****	***	1.100	1
5	Inner box bag	*****	***	***	***
6	Total weight	7.54 Kg		± 5%	

7.1.2 Specification and quantity

Modules x tray	Quantity per row	6	x	Quantity per column	7	=	42
Modules per box	Quantity per tray	42	x	Quantity of trays	15	=	630
Total no. of modules	Quantity per box	630	x	Quantity of boxes	4	=	2520







7.2 LABELLING & MARKING

DENSITRON DD-9664FC-2A TW YY MM

8 QUALITY ASSURANCE SPECIFICATION

8.1 CONFORMITY

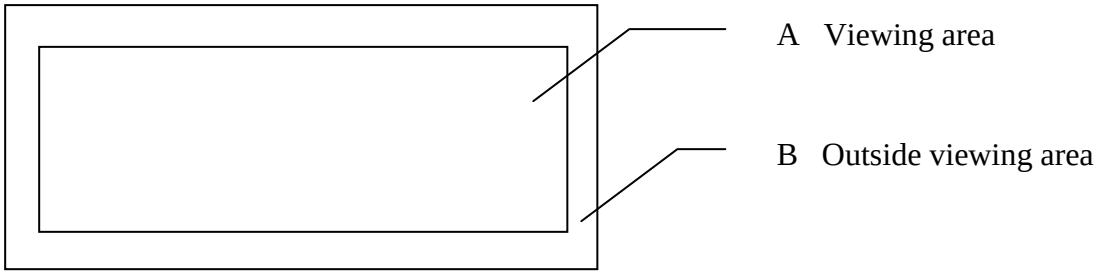
The performance, function and reliability of the shipped products conform to the Product Specification.

8.2 DELIVERY ASSURANCE

8.2.1 Delivery inspection standards

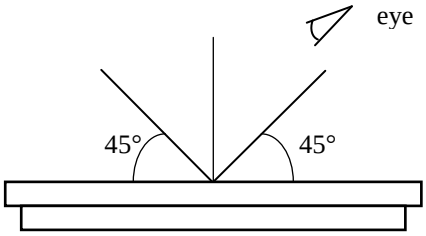
- IPC-AA610 rev. C, class 2 electronic assemblies standard

8.2.2 Zone definition



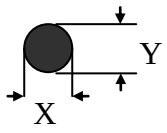
8.2.3 Visual inspection

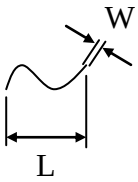
- Inspect under 30W fluorescent lamp leaving 50 cm between the module and the lamp and 30 cm between the module and the eye (measuring position).
- Appearance is inspected at the best contrast voltage (best contrast is adjusted considering clearness and crosstalk on screen).
- Inspect the module at 45° right and left, top and bottom.
- Use the optimum viewing angle during the contrast inspection.

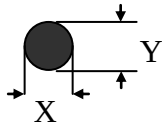


8.2.4 Standard of appearance inspection

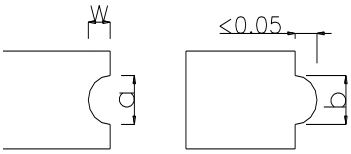
Units: mm

<table>
<tr><th>Class</th><th>Item</th><th>Criteria</th></tr>
<tr><td>Minor</td><td rowspan="2">Packing & Label</td><td>Outside & inside package | Presence of product no., lot no., quantity</td></tr>
<tr><td>Critical</td><td>Product must not be mixed with others and quantity must not be different from that indicated on the label</td></tr>
<tr><td>Major</td><td>Dimension</td><td>Product dimensions must be according to specification and drawing</td></tr>
<tr><td>Major</td><td>Electrical</td><td>Product electrical characteristics must be according to specification</td></tr>
<tr><td>Critical</td><td>OLED Display</td><td>Missing lines or wrong patterns on display are not allowed</td></tr>
<tr><td>Minor</td><td>Black spot, white spot, dust</td><td>Round type: as per following drawing
∅ = (X+Y)/2
 

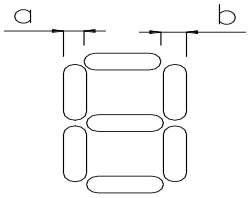
<table><tr><th colspan="3">Acceptable quantity</th></tr><tr><th>Size</th><th>Zone A</th><th>Zone B</th></tr><tr><td>∅<0.1</td><td>Any number</td><td rowspan="4">Any number</td></tr><tr><td>0.1<∅<0.2</td><td>3</td></tr><tr><td>0.2<∅<0.25</td><td>1</td></tr><tr><td>0.25<∅</td><td>0</td></tr></table>
Line type: as per following drawing
 

<table><tr><th colspan="4">Acceptable quantity</th></tr><tr><th>Length</th><th>Width</th><th>Zone A</th><th>Zone B</th></tr><tr><td>- -</td><td>W≤0.05</td><td>Any number</td><td rowspan="3">Any number</td></tr><tr><td>L≤2.0</td><td>W≤0.1</td><td>3</td></tr><tr><td>L>2.0</td><td></td><td>0</td></tr></table>
Total acceptable quantity: 3</td></tr>
<tr><td>Minor</td><td>Polariser scratch</td><td>Scratch on protective film is permitted
Scratch on polariser: same as No. 1</td></tr>
<tr><td>Minor</td><td>Polariser bubble</td><td>∅ = (X+Y)/2
 

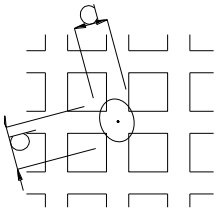
<table><tr><th colspan="3">Acceptable quantity</th></tr><tr><th>Size</th><th>Zone A</th><th>Zone B</th></tr><tr><td>∅<0.5</td><td>Any number</td><td rowspan="2">Any number</td></tr><tr><td>∅>0.5</td><td>0</td></tr></table>
Total acceptable quantity: 3</td></tr>
</table>

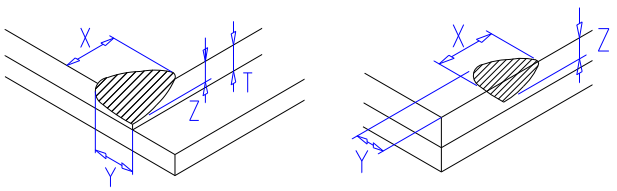
<table>
<tr><th>Class</th><th>Item</th><th>Criteria</th></tr>
<tr><td>Minor</td><td>Segment deformation</td><td>
1b. Pin hole on dot matrix display


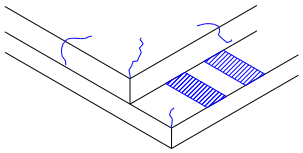
<table>
<tr><td colspan="2">Acceptable quantity</td></tr>
<tr><td>Size</td><td></td></tr>
<tr><td>a,b<0.1</td><td>Any number</td></tr>
<tr><td>(a+b)/2≤0.1</td><td>Any number</td></tr>
<tr><td>0.5<∅<1.0</td><td>3</td></tr>
</table>
Total acceptable quantity: 7

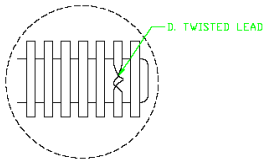
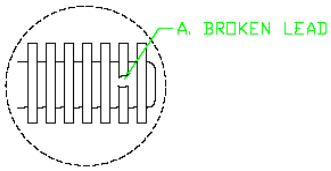
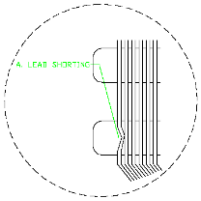
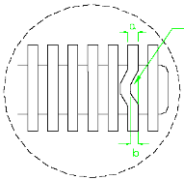
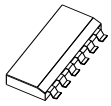
2. Segments / dots with different width


<table>
<tr><td colspan="2">Acceptable</td></tr>
<tr><td>a≥b</td><td>a/b≤4/3</td></tr>
<tr><td>a<b</td><td>a/b>4/3</td></tr>
</table>

3. Alignment layer defect
∅ = (a+b)/2


<table>
<tr><td colspan="2">Acceptable quantity</td></tr>
<tr><td>Size</td><td></td></tr>
<tr><td>∅≤0.4</td><td>Any number</td></tr>
<tr><td>0.4<∅≤1.0</td><td>5</td></tr>
<tr><td>1.0<∅≤1.5</td><td>3</td></tr>
<tr><td>1.5<∅≤2.0</td><td>2</td></tr>
</table>
Total acceptable quantity: 7
</td></tr>
<tr><td>Minor</td><td>Panel Chipping</td><td>
X ≤ 1/6 Panel length
Y ≤ 1
Z ≤ T


</td></tr>
<tr><td>Minor</td><td>Panel Cracking</td><td>
Cracks not allowed

</td></tr>
<tr><td>Minor</td><td>Cupper exposed (pin or film)</td><td>Not allowed if visible by eye inspection</td></tr>
<tr><td>Minor</td><td>Film or Trace Damage</td><td>Not allowed if affects electrical function</td></tr>
</table>

<table>
<tr><th>Class</th><th>Item</th><th>Criteria</th></tr>
<tr><td>Minor</td><td>Contact
Lead Twist</td><td>Not allowed
  </td></tr>
<tr><td>Minor</td><td>Contact
Lead
Broken</td><td>Not allowed
  </td></tr>
<tr><td rowspan="2">Minor</td><td rowspan="2">Contact
Lead Bent</td><td>Not allowed if
bent lead causes
short circuit
  </td></tr>
<tr><td>Not allowed if bent lead
extends horizontally
more than 50%
of its width
  </td></tr>
<tr><td>Minor</td><td>Colour
uniformity</td><td>Level of sample for approval set as limit sample</td></tr>
<tr><td>Major</td><td rowspan="4">PCB
  </td><td>No unmelted solder paste should be present on PCB</td></tr>
<tr><td>Critical</td><td>Cold solder joints, missing solder connections, or oxidation are not allowed</td></tr>
<tr><td>Minor</td><td>No residue or solder balls on PCB are allowed</td></tr>
<tr><td>Critical</td><td>Short circuits on components are not allowed</td></tr>
<tr><td>Minor</td><td>Tray
particles</td><td>
<table>
<tr><th></th><th>Size</th><th>Quantity</th></tr>
<tr><td rowspan="2">On tray</td><td>∅<0.2</td><td>Any number</td></tr>
<tr><td>∅>0.25</td><td>4</td></tr>
<tr><td rowspan="2">On display</td><td>∅≥0.25</td><td>2</td></tr>
<tr><td>L = 3</td><td>1</td></tr>
</table>
</td></tr>
</table>

8.3 DEALING WITH CUSTOMER COMPLAINTS

8.3.1 Non-conforming analysis

Purchaser should supply Densitron with detailed data of non-conforming sample.
After accepting it, Densitron should complete the analysis in two weeks from receiving the sample.
If the analysis cannot be completed on time, Densitron must inform the purchaser.

8.3.2 Handling of non-conforming displays

If any non-conforming displays are found during customer acceptance inspection which Densitron is clearly responsible for, return them to Densitron.
Both Densitron and customer should analyse the reason and discuss the handling of non-conforming displays when the reason is not clear.
Equally, both sides should discuss and come to agreement for issues pertaining to modification of Densitron quality assurance standard.

9 RELIABILITY SPECIFICATION

9.1 CONTENTS OF RELIABILITY TESTS

Test Item	Test Condition	Evaluation and assessment
High Temperature Operation	70°C±2, 240 hours	No abnormalities in function and appearance
Low Temperature Operation	-30°C±2, 240 hours	No abnormalities in function and appearance
High Temperature Storage	80°C±2, 240 hours	No abnormalities in function and appearance
Low Temperature Storage	-40°C±2, 240 hours	No abnormalities in function and appearance
High Temperature & High Humidity Operation	60°C, 90%RH, 120 hours	No abnormalities in function and appearance
Thermal Shock	24 cycles of -40°C to 85°C, 1 hour dwell	No abnormalities in function and appearance

* The samples used for the above tests do not include polarizer.
* No moisture condensation is observed during tests.

9.2 FAILURE CHECK STANDARD

After the completion of the described reliability test, the samples wewe left at room temperature for 2 hrs prior to conducting the failure teat at 23±5 °C；55±15% RH.

9.3 LIFE TIME

Item	Description
1	Function, performance, appearance, etc. shall be free from remarkable deterioration more than 10,000 hours under ordinary operating and storage conditions of room temperature (25±10 °C), normal humidity (45±20% RH), and in area not exposed to direct sunlight.
2	End of lifetime is specified as 50% of initial brightness.

10 HANDLING PRECAUTIONS

Safety
If the panel breaks, be careful not to get the organic substance in your mouth or in your eyes.
If the organic substance touches your skin or clothes, wash it off immediately using soap and plenty of water.

Mounting and Design
Place a transparent plate (e.g. acrylic, polycarbonate or glass) on the display surface to protect the display from external pressure. Leave a small gap between the transparent plate and the display surface.
Design the system so that no input signal is given unless the power supply voltage is applied.

Caution during OLED cleaning
Lightly wipe the display surface with a soft cloth soaked with Isopropyl alcohol, Ethyl alcohol or Trichlorotriflorothane.
Do not wipe the display surface with dry or hard materials that will damage the polariser surface.
Do not use aromatic solvents (toluene and xylene), or ketonic solvents (ketone and acetone).

Caution against static charge
As the display uses C-MOS LSI drivers, connect any unused input terminal to V_{DD} or V_{SS}. Do not input any signals before power is turned on.
Also, ground your body, work/assembly table and assembly equipment to protect against static electricity.

Packaging
Displays use OLED elements, and must be treated as such. Avoid strong shock and drop from a height.
To prevent displays from degradation, do not operate or store them exposed directly to sunshine or high temperature/humidity.

Caution during operation
It is indispensable to drive the display within the specified voltage limit since excessive voltage shortens its life.

Other Precautions
When a display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur.
Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored.
Also, there will be no problem in the reliability of the module.

Storage
Store the display in a dark place where the temperature is 25°C ± 10°C and the humidity below 50%RH.
Store the display in a clean environment, free from dust, organic solvents and corrosive gases.
Do not crash, shake or jolt the display (including accessories).

11 SUPPORTED ACCESSORIES

11.1 DUO KIT

Densitron has developed an easy to use yet powerful development and demonstration tool for driving its range of Passive Matrix OLED displays from the USB port of a PC.
DUO (Densitron USB OLED) kit is hot pluggable and does not require extra cables or power supply to run, allowing users to be up and running in minutes.

The kit consists of an OLED display with transition Board, USB controller card, mini USB cable and a CD with software application and drivers.

Part number: PDK-N-9664FC-2A

11.2 TRANSITION BOARD CARD

A Transition board card is like a daughterboard which is meant to be a circuit board for connections between the baseboards (DUO).
It has connector pins for interfacing between the display and the baseboards.
It also includes the OLED display.
Part number: PDT-N-9664FC-2A

11.3 CONNECTOR BOARD CARD

A Connector board card is also a daughterboard which is a circuit board for connection between a microprocessor or microcontroller (customer's system).

Part number: EVK-CONNECT-018

11.4 CONNECTOR

Type: hot bar soldering process
No. of connections: 23
Pitch: 0.70mm