DENSITRON DISPLAYS

OLED DISPLAY MODULE

Product Specification

CUSTOMER	**Standard**	
PRODUCT NUMBER	**DD-9639BE-4A**	
CUSTOMER APPROVAL		**Date**

INTERNAL APPROVALS		
Product Mgr	Doc. Control	Electr. Eng
Bazile Peter	**Bazile Peter**	**Luo Luo**
Date: 26/09/11	Date: 26/09/11	Date: 26/09/11

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REVISION RECORD

Rev.	Date	Page	Chapt.	Comment	ECR no.
A	27 Sep11			First Issue	
B	28 Nov 12	36	10	Update the connector information	

1 MAIN FEATURES

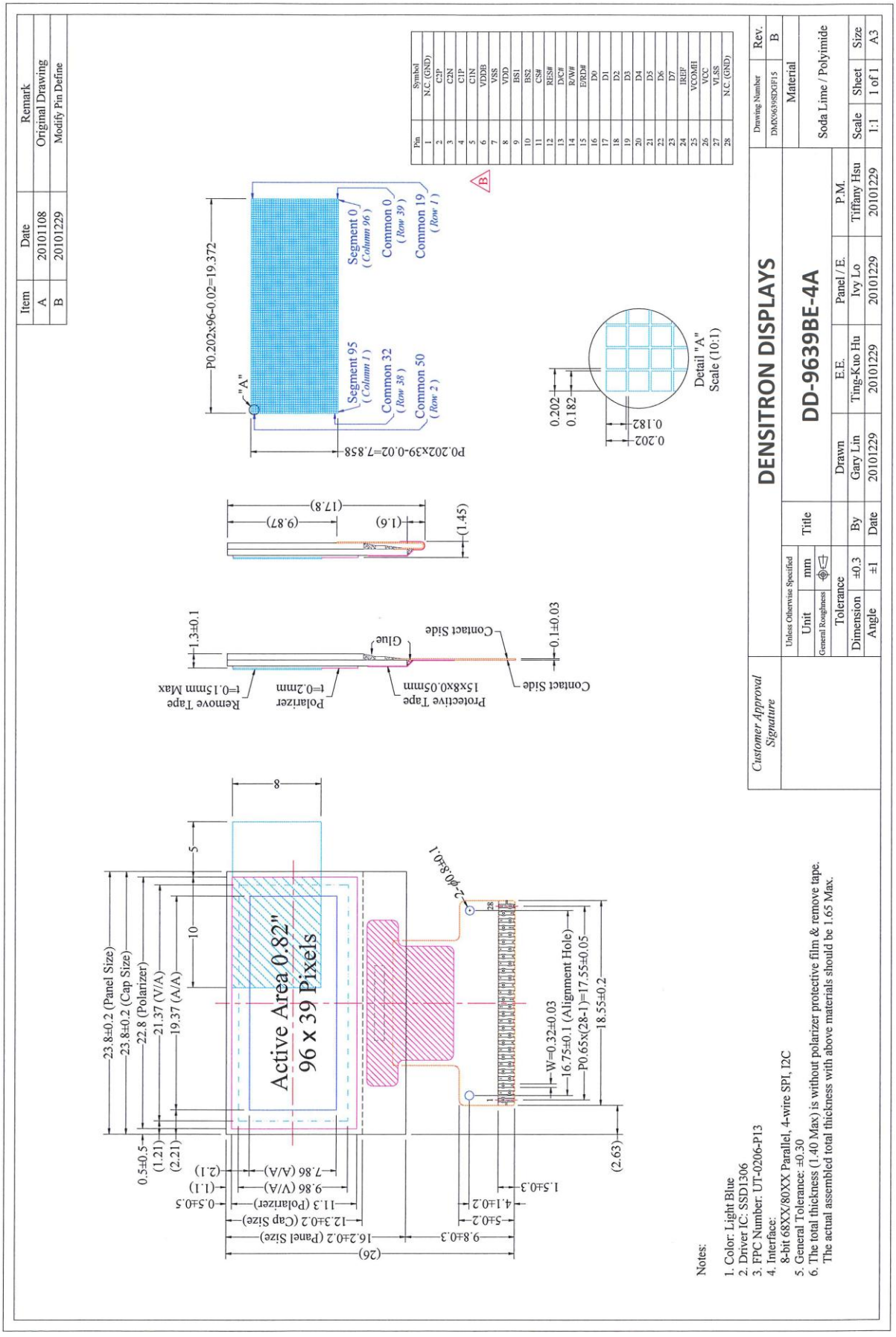
ITEM	CONTENTS
Display Format	96 x 39 Dots
Overall Dimensions(W*H*T)	23.80×16.20× 1.30 mm
Active Area(W*H)	19.372 × 7.858 mm
Viewing Area(W*H)	21.372 x 9.858 mm
Display Mode	Passive Matrix
Display Colour	Blue Colour
Driving Method	1 / 39 duty
Driver IC	SSD1306
Operating temperature	-30℃ ~ +70℃
Storage temperature	-40℃ ~ +85℃

2 MECHANICAL SPECIFICATION

2.1 MECHANICAL CHARACTERISTICS

ITEM	CHARACTERISTIC	UNIT
Display Format	96 x 39	Dots
Overall Dimensions	23.80×16.20× 1.30	mm
Viewing Area	21.372 x 9.858	mm
Active Area	19.372 × 7.858	mm
Dot Size	0.182 × 0.182	mm
Dot Pitch	0.202 × 0.202	mm
Weight	0.99	g
IC Controller/Driver	SSD1306	

2.2 MECHANICAL DRAWING



3 ELECTRICAL SPECIFICATION

3.1 ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min	Max	Unit	Note
Supply Voltage for Logic	V_{DD}	-0.3	4	V	Note 1, 2
Supply Voltage for Display	V_{CC}	0	11	V	Note 1, 2
Supply Voltage for DC/DC	V_{DDB}	-0.3	5	V	Note 1, 2
Operating Temperature	Top	-40	70	°C	Note 3
Storage Temperature	Tstg	-40	85	°C	Note 4

Note 1: All the above voltages are on the basis of "VSS=0V".

Note 2: When this module is used beyond above absolute maximum ratings, permanent damage to the module may occur. Also for normal operations it's desirable to use this module under the conditions according to Section 3.2 "Electrical Characteristics" and section 4 "optical characteristic. If this module is used beyond these conditions the module may malfunction and the reliability could deteriorate.

Note 3: the defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80 °C

Note 4: VCC=7.25V, Ta=25°C, 50% checkerboard.
Software configuration follows Section 5.4 initialization.
End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions

3.2 ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Logic	VDD	Ta = 25°C	1.65	2.8	3.3	V
Supply Voltage for Display (external)	VCC	Ta = 25°C Note 4	7	7.25	7.5	V
Supply Voltage for DC/DC	VDDB	Internal DC/DC	3.3		4.2	V
Supply Voltage for Display (Generated by Internal DC/DC)	VCC	Note 3	7	-	7.5	V
High Level Input	VIH		0.8xVDD	-	VDD	V
Low Level Input	VIL		0	-	0.2xVDD	V
High Level Output	VOH	Iout=100µA,3.3MHz	0.9xVDD	-	VDD	V
Low Level Output	VOL	Iout=100µA,3.3MHz	0	-	0.1xVDD	V
Operating Current for VDD	IDD	Note 1		180	300	µA
Operating Current for VCC	ICC	Note 1		2.3	2.9	mA
		Note 2		3.6	4.5	mA
		Note 3		7.2	9.0	mA
Operating Current for VDDB(VCC Generated by Internal DC/DC)	IBAT	Note 1		6.9	8.6	mA
		Note 2		10.9	13.6	mA
		Note 3		20.8	26.0	mA
Sleep Mode Current for VCI	IDD, SLEEP			1	5	µA
Sleep Mode Current for VCC	ICC, SLEEP			2	10	µA

Note 1 V_{DD}= 2.8V, V_{CC} = 7.25V, 30% Display area turned on.
Note 2 2.8V, V_{CC} = 7.25V, 50% Display area V_{DD} =turned on
Note 3 2.8V, V_{CC} = 7.25V, 100% Display area V_{DD} =turned on
Note 4 Brightness (L_{br}) and Supply Voltage for Display (V_{CC}) are subject to the change of the panel characteristics.

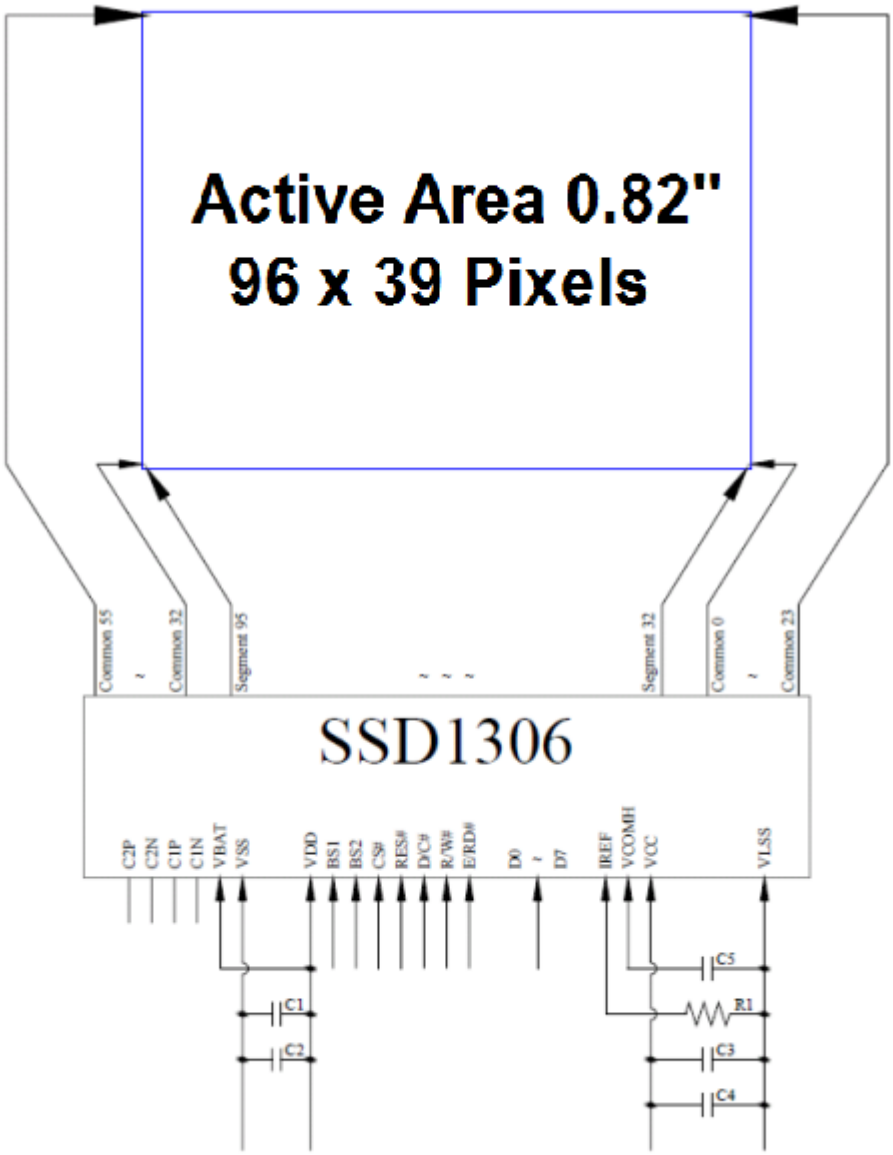
3.3 INTERFACE PIN ASSIGNMENT

<table>
<tr><th>No.</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>1</td><td>N.C. (GND)</td><td>-</td><td>Reserved Pin (Supporting Pin)
The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground.</td></tr>
<tr><td>2</td><td>C2P</td><td>I</td><td rowspan="4">Positive Terminal of the Flying Inverting Capacitor
Negative Terminal of the Flying Boost Capacitor
The charge-pump capacitors are required between the terminals. They must be floated when the inbuilt DC-DC converter is not used.</td></tr>
<tr><td>3</td><td>C2N</td><td>I</td></tr>
<tr><td>4</td><td>C1P</td><td>I</td></tr>
<tr><td>5</td><td>C1N</td><td>I</td></tr>
<tr><td>6</td><td>VDDB</td><td>P</td><td>Power Supply for DC/DC Converter Circuit
This is the power supply pin for the internal buffer of the DC/DC voltage converter. It must be connected to external source when the converter is used. It should be connected to VDD when the converter is not used.</td></tr>
<tr><td>7</td><td>VSS</td><td>P</td><td>Ground of Logic Circuit
This is a ground pin. It acts as a reference for the logic pins. It must be connected to external ground.</td></tr>
<tr><td>8</td><td>VDD</td><td>P</td><td>Power Supply for Logic
This is a voltage supply pin. It must be connected to external source</td></tr>
<tr><td>9</td><td>BS1</td><td rowspan="2">I</td><td rowspan="2">Communicating Protocol Select
These pins are MCU interface selection input. See the following table:
<table><tr><th></th><th>BS1</th><th>BS2</th></tr><tr><td>I2C</td><td>1</td><td>0</td></tr><tr><td>4-wire SPI</td><td>0</td><td>0</td></tr><tr><td>8 bit 68XX-parallel</td><td>0</td><td>1</td></tr><tr><td>8 bit 80XX-parallel</td><td>1</td><td>1</td></tr></table></td></tr>
<tr><td>10</td><td>BS2</td></tr>
<tr><td>11</td><td>CS#</td><td>I</td><td>Chip Select
This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.</td></tr>
<tr><td>12</td><td>RES#</td><td>I</td><td>Power Reset for Controller and Driver
This pin is reset signal input. When the pin is low, initialization of the chip is executed.</td></tr>
</table>

13	D/C#	I	Data/Command Control This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 is treated as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams. When the pin is pulled high and serial interface mode is selected, the data at SDIN is treated as data. When it is pulled low, the data at SDIN will be transferred to the command register. In I2C mode, this pin acts as SA0 for slave address selection.
14	R/W#	I	Read/Write Select or Write This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to "High" for read mode and pull it to "Low" for write mode. When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low.
15	E/RD#	I	Read/Write Enable or Read This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low. When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low.
16~23	D0~D7	I/O	Host Data Input/output Bus These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK. When I2C mode is selected, D2 & D1 should be tired together and serve as SDAout & SDAin in application and D0 is the serial clock input SCL.
24	IREF	I	Current Reference for Brightness Adjustment This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current lower than 12.5μA maximum.
25	VCOMH	O	Voltage Output High Level for COM Signal This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and VSS.
26	VCC	P	Power Supply for OEL Panel This is the most positive voltage supply pin of the chip. A stabilization capacitor should be connected between this pin and VSS when the converter is used. It must be connected to external source when the converter is not used.
27	VLSS		Ground of Analogue Circuit This is an analogue ground pin. It should be connected to VSS externally.
28	N.C. (GND)	-	Reserved Pin (Supporting Pin) The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground.

3.4 BLOCK DIAGRAM

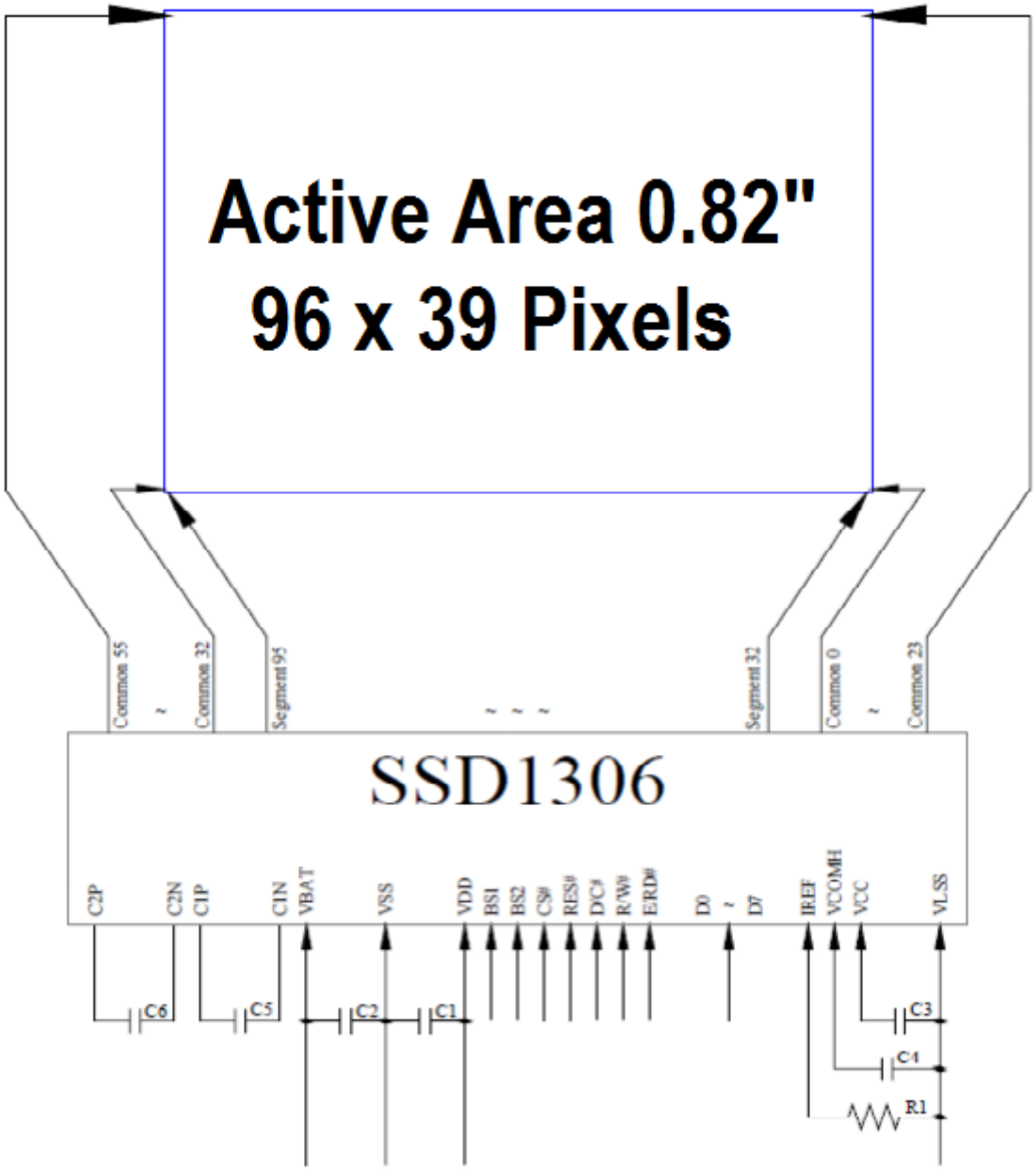
3.4.1 VCC SUPPLIED EXTERNAL



MCU Interface Selection: BS1 and BS2
Pins connected to MCU interface: CS#, RES#, D/C#, R/W#, E/RD#, and D0~D7

C1, C3:	0.1µF
C2:	2.2 µF
C4, C5:	4.7 µF/16V, X7R
R1:	390kΩ, R1 = (Voltage at IREF – VSS) / IREF

3.4.1 VCC SUPPLIED using internal DC/DC



MCU Interface Selection: BS1 and BS2
Pins connected to MCU interface: CS#, RES#, D/C#, R/W#, E/RD#, and D0~D7

C1, C2, C5, C6: 1µF
C3: 2.2 µF
C4: 4.7 µF/16V, X7R
R1: 390kΩ, R1 = (Voltage at IREF – VSS) / IREF

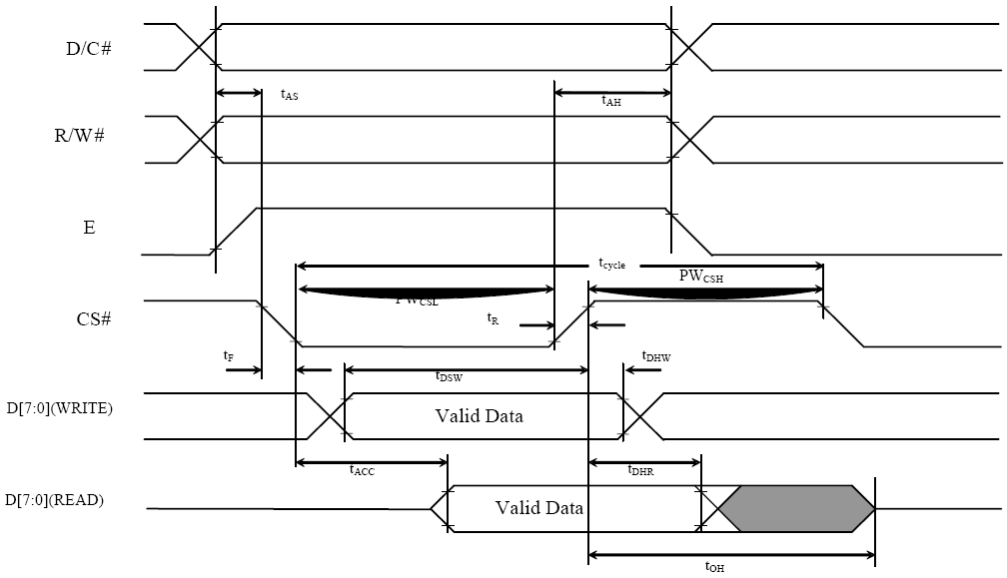
3.5 CHARACTERISTICS

3.5.1 AC CHARACTERISTICS

3.5.2 68XX-Series MPU Parallel Interface Timing Characteristics

Characteristics	Symbol	Min	Max	Unit
Clock Cycle Time	t_{cycle}	300	-	ns
Address Setup Time	t_{AS}	0	-	ns
Address Hold Time	t_{AH}	0	-	ns
Write Data Setup Time	t_{DSW}	40	-	ns
Write Data Hold Time	t_{DHW}	7	-	ns
Read Data Hold Time	t_{DHR}	20	-	ns
Output Disable Time	t_{OH}	-	70	ns
Access Time	t_{ACC}	-	140	ns
Chip Select Low Pulse Width (Read) Chip Select Low Pulse Width (Write)	PW_{CSL}	120 60	-	ns
Chip Select High Pulse Width (Read) Chip Select High Pulse Width (Write)	PW_{CSH}	60 60	-	ns
Rise Time	t_R	-	40	ns
Fall Time	t_F	-	40	ns

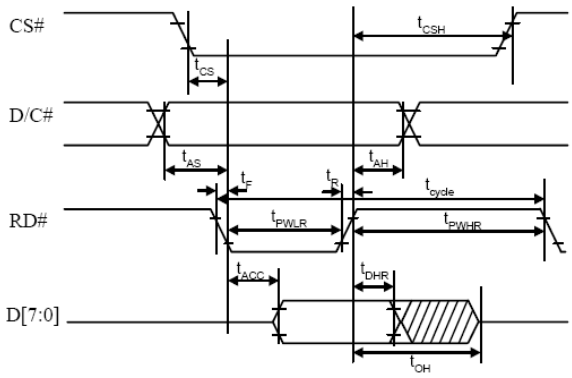
(V_{DD} - V_{SS} = 1.65V, V_{CI} = 3.3V, T_a = 25°C)



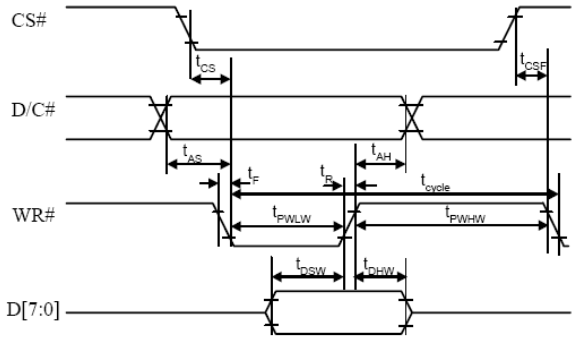
3.5.3 8080-Series MPU Parallel Interface Timing Characteristics

Characteristics	Symbol	Min	Max	Unit
Clock Cycle Time	t_{cycle}	300	-	ns
Address Setup Time	t_{AS}	10	-	ns
Address Hold Time	t_{AH}	0	-	ns
Write Data Setup Time	t_{DSW}	40	-	ns
Write Data Hold Time	t_{DHW}	7	-	ns
Read Data Hold Time	t_{DHR}	20	-	ns
Output Disable Time	t_{OH}	-	70	ns
Access Time	t_{ACC}	-	140	ns
Read Low Time	t_{PWLR}	120	-	ns
Write Low Time	t_{PWLW}	60	-	ns
Read High Time	t_{PWHR}	60	-	ns
Write High Time	t_{PWHW}	60	-	ns
Chip Select Setup Time	t_{CS}	0	-	ns
Chip Select Hold Time to Read Signal	t_{CSH}	0	-	ns
Chip Select Hold Time	t_{CSF}	20	-	ns
Rise Time	t_R	-	40	ns
Fall Time	t_F	-	40	ns

(V_{DD} - V_{SS} 1.65V to 3.3V, T_a = 25°C)



Read Timing

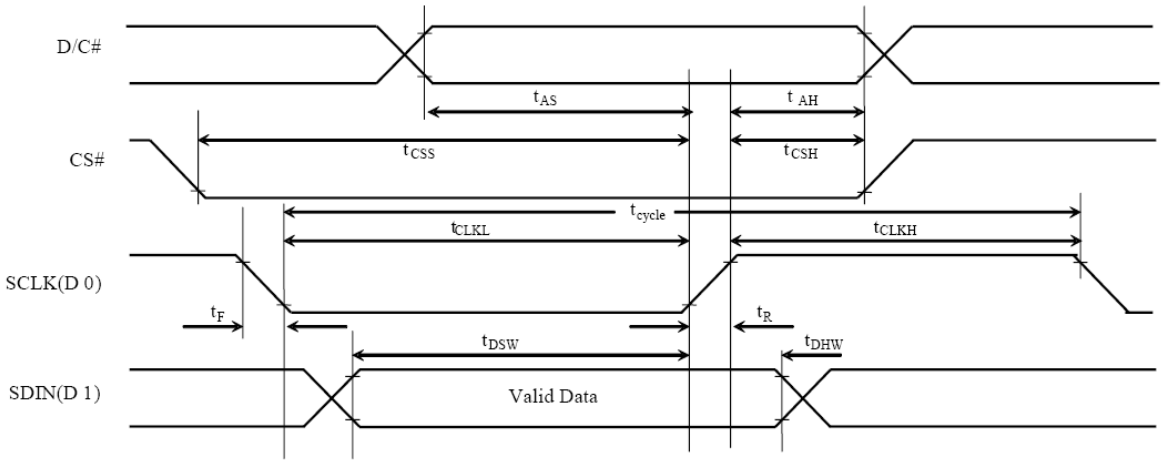


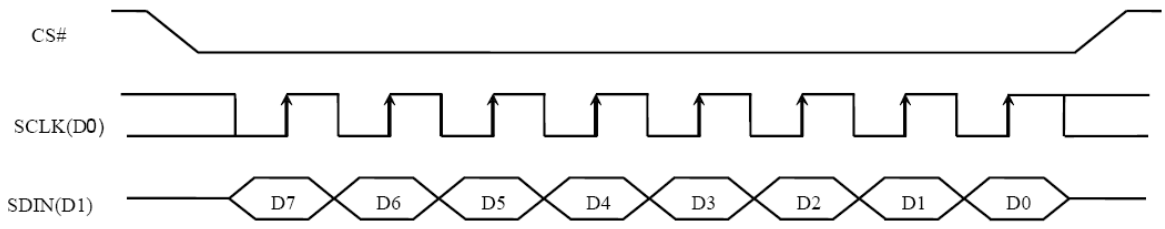
Write Timing

3.5.4 Serial Interface Timing Characteristics (4-wire SPI)

Characteristics	Symbol	Min	Max	Unit
Clock Cycle Time	t_{cycle}	100	-	ns
Address Setup Time	t_{AS}	15	-	ns
Address Hold Time	t_{AH}	15	-	ns
Chip Select Setup Time	t_{CSS}	20	-	ns
Chip Select Hold Time	t_{CSH}	10	-	ns
Write Data Setup Time	t_{DSW}	15	-	ns
Write Data Hold Time	t_{DHW}	15	-	ns
Clock Low Time	t_{CLKL}	20	-	ns
Clock High Time	t_{CLKH}	20		ns
Rise Time	t_R	-	40	ns
Fall Time	t_F	-	40	ns

(VDD – VSS = 1.6V to 3.3V, Ta = 25°C)

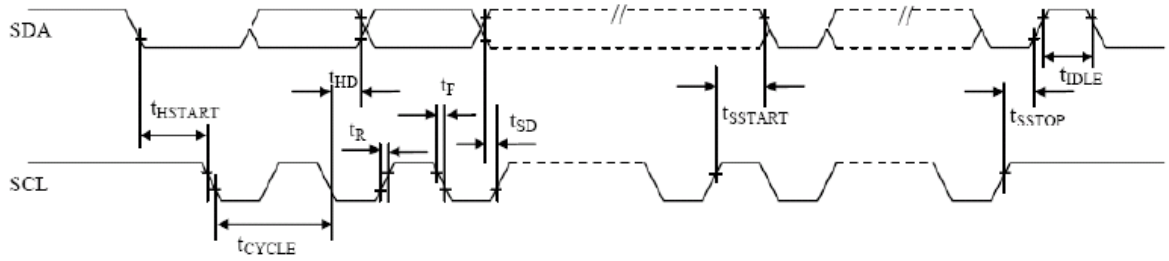




3.5.5 I2C Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	us
t_{HSTART}	Start Condition Hold Time	0.6	-	us
t_{HD}	Data Hold Time (for "SDA_{OUT}" Pin)	0	-	ns
	Data Hold Time (for "SDA_{IN}" Pin)	300		
t_{SD}	Data Setup Time	100	-	ns
t_{SSTART}	Start Condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	us
t_{SSTOP}	Stop Condition Setup Time	0.6	-	us
t_R	Rise Time for Data and Clock Pin		300	ns
t_F	Fall Time for Data and Clock Pin		300	ns
t_{IDLE}	Idle Time before a New Transmission can Start	1.3	-	us

* (V_{DD} - V_{SS} = 1.65V to 3.3V, T_a = 25°C)



4 OPTICAL SPECIFICATION

4.1 OPTICAL CHARACTERISTICS

Characteristics	Symbol	Condition	Min	Typ	Max	Unit
Brightness	L_{br}	With Polarizer Note 1	80	100	-	cd/m^2
C.I.E.(BLUE)	(X)	C.I.E. 1931	0.12	0.16	0.20	-
	(Y)		0.22	0.26	0.30	
Dark Room Contrast	CR		-	>10000:1	-	-
Viewing Angle			-	Free	-	degree

Optical measurement taken at V_{DD} = 2.8V, V_{CC} = 7.25V
Software configuration follows Section 5.4 Initialization.

5 FUNCTIONAL SPECIFICATION

5.1 COMMANDS

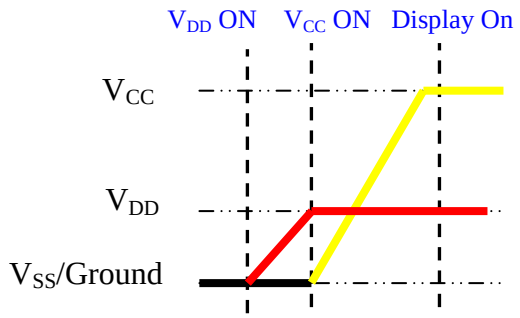
Please refer to the Technical Manual for the SSD1306

5.2 POWER UP/DOWN SEQUENCE

To protect panel and extend the panel lifetime, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the panel enough time to complete the action of charge and discharge before/after the operation.

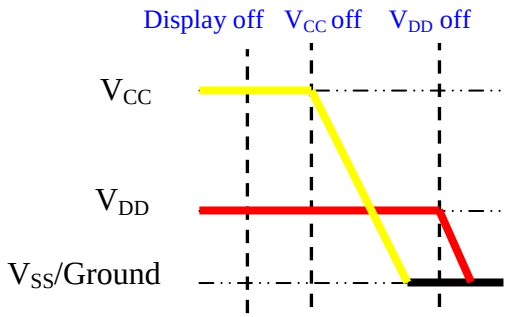
5.2.1 POWER UP SEQUENCE

1. Power up V_{DD}
2. Send Display off command
3. Initialization 4. Clear Screen
5. Power up V_{CC}
6. Delay 100ms
   (When V_{CC} is stable)
7. Send Display on command



5.2.2 POWER DOWN SEQUENCE

1. Send Display off command
2. Power down V_{CC}
3. Delay 100ms
   (When V_{CC} is reach 0 and panel is completely discharges)
4. Power down V_{DD}



1) Since an ESD protection circuit is connected between VDD and VCC inside the driver IC, VCC becomes lower than VDD whenever VDD is ON and VCC is OFF.
2) VCC should be kept float (disable) when it is OFF.
3) Power Pins (VDD, VCC) can never be pulled to ground under any circumstance.
4) VDD should not be power down before VCC power down.

5.3 RESET CIRCUIT

When RES# input is low, the chip is initialized with the following status:

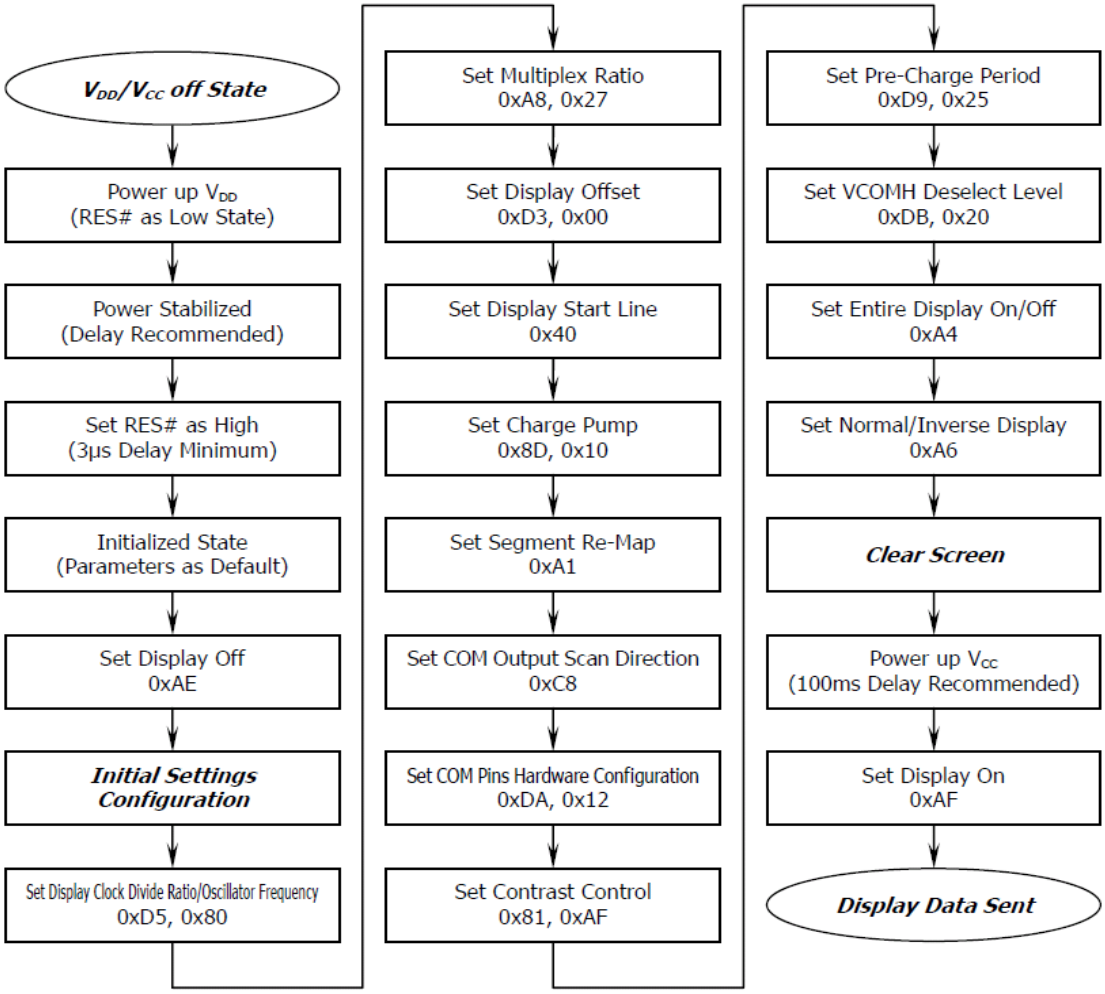
1. Display is off
2. 128×64 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 7Fh
9. Normal display mode (Equivalent to A4h command)

5.4 ACTUAL APPLICATION EXAMPLE

Command usage and explanation of an actual example

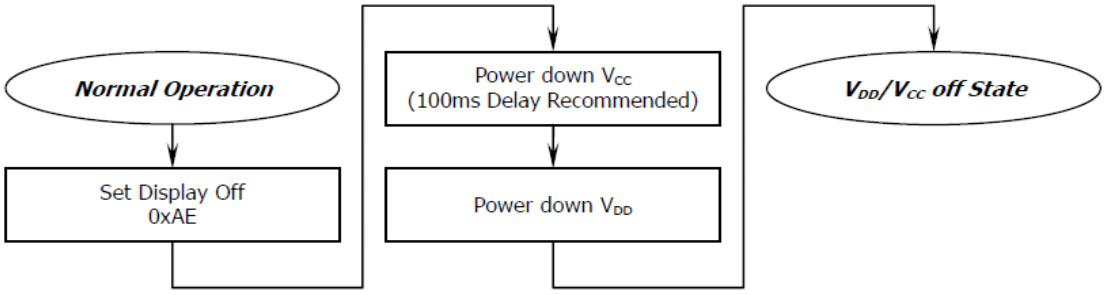
5.4.1 VCC Supplied Externally

<Power up Sequence>

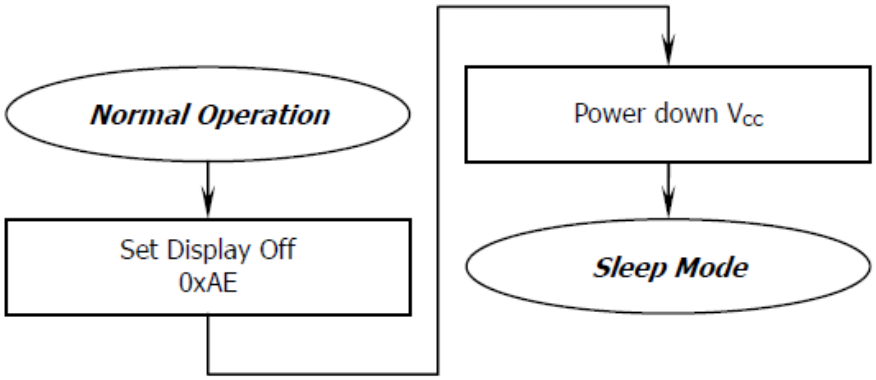


If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

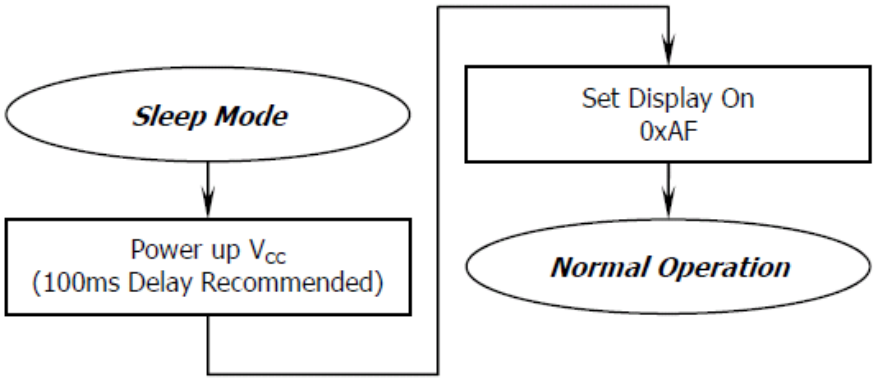
<Power down Sequence>



<Entering Sleep Mode>

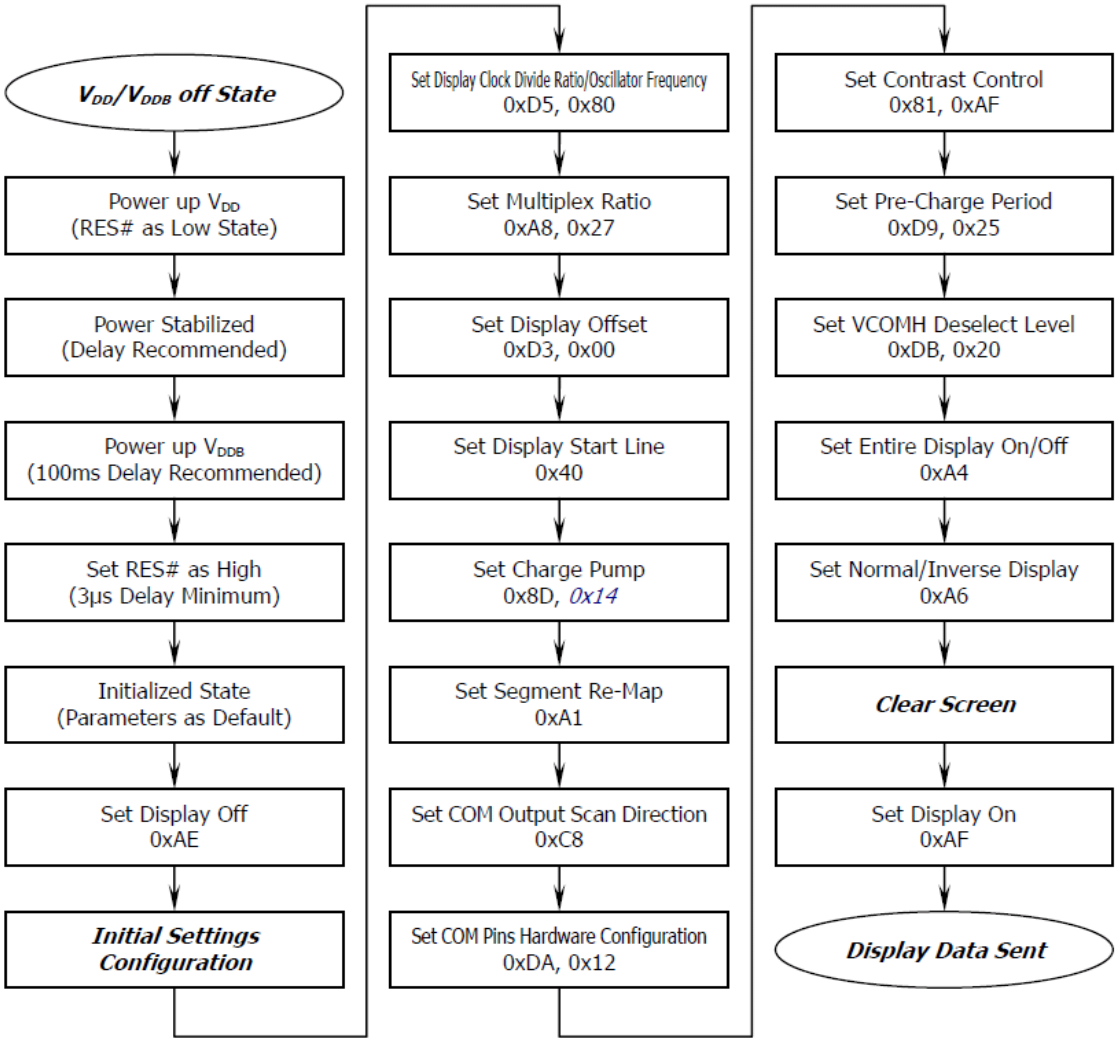


<Exiting Sleep Mode>



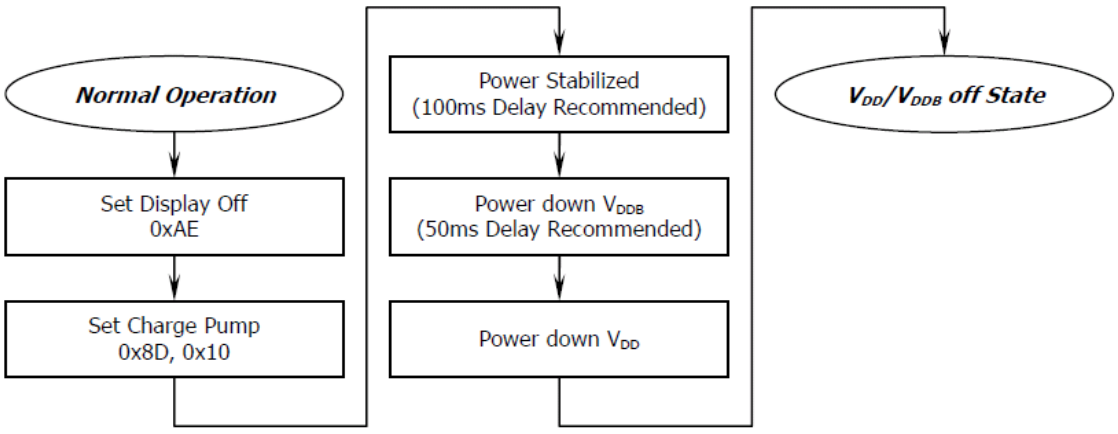
5.4.2 VCC Generated by Internal DC/DC Circuit

<Power up Sequence>

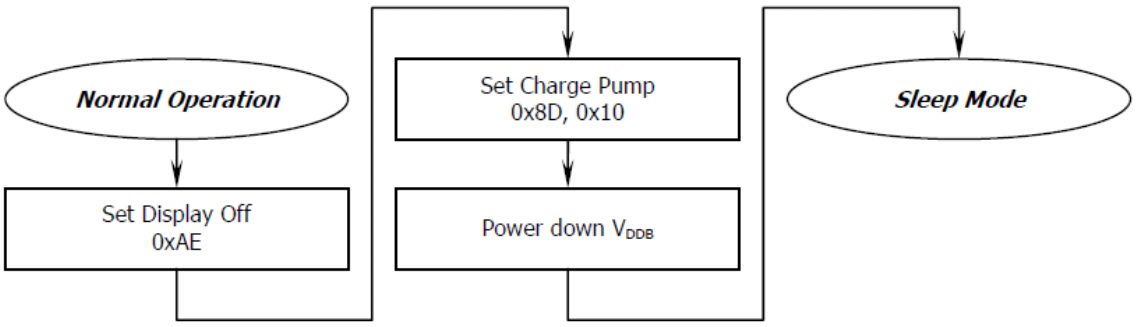


If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

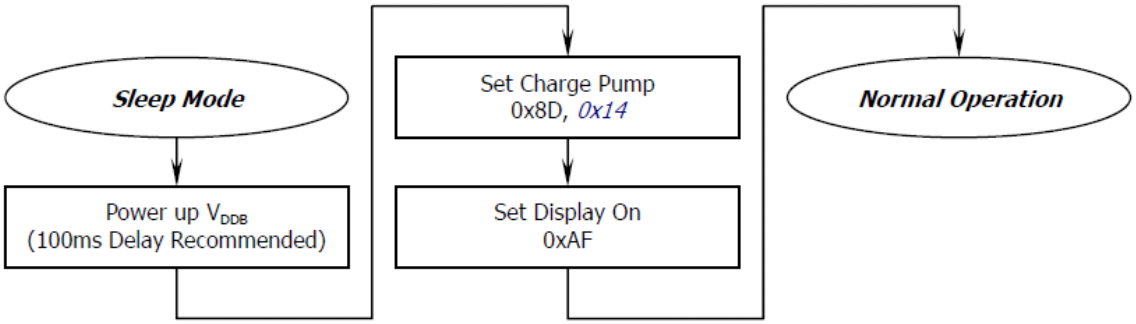
<Power down Sequence>



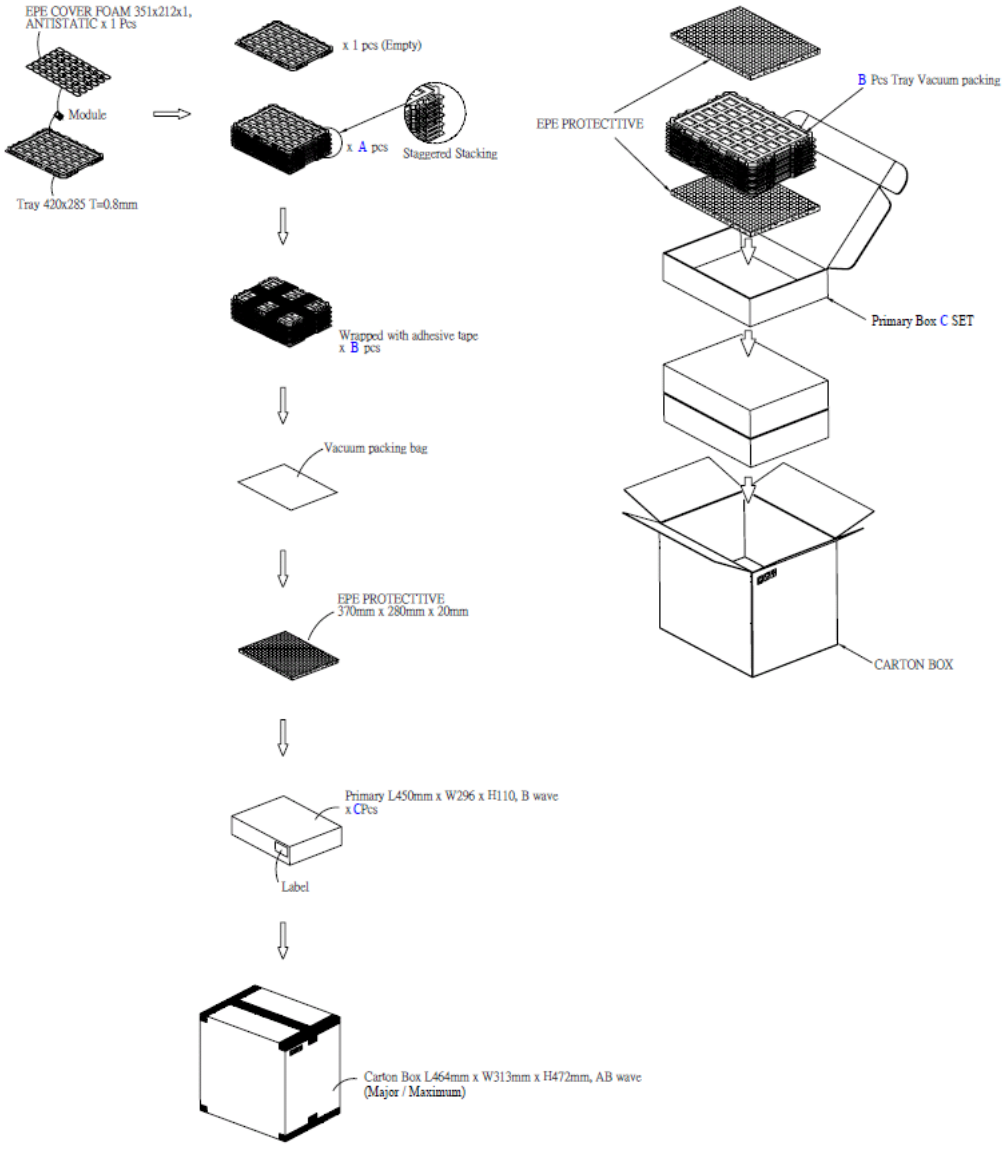
<Entering Sleep Mode>



<Exiting Sleep Mode>



6 PACKAGING AND LABELLING SPECIFICATION



Item		Quantity	
Holding Trays	(A)	15	per Primary Box
Total Trays	(B)	16	per Primary Box (Including 1 Empty Tray)
Primary Box	(C)	1~4	per Carton (4 as Major / Maximum)

6.1 LABELLING & MARKING

DENSITRON
DD-9639BE-4A
TW YY MM

7 QUALITY ASSURANCE SPECIFICATION

7.1 CONFORMITY

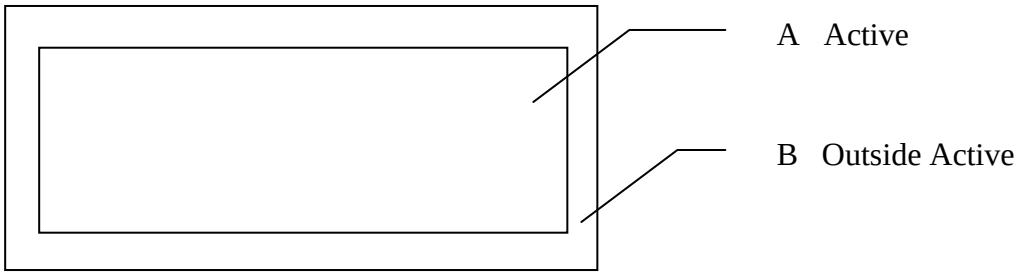
The performance, function and reliability of the shipped products conform to the Product Specification.

7.2 DELIVERY ASSURANCE

7.2.1 DELIVERY INSPECTION STANDARDS

IPC-AA610, class 2 electronic assemblies standard

7.2.2 Zone definition



7.2.3 Visual inspection

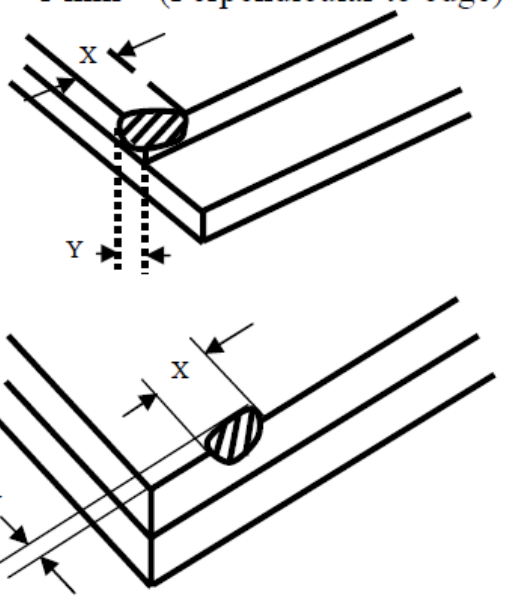
Test and measurement to be conducted under following conditions：

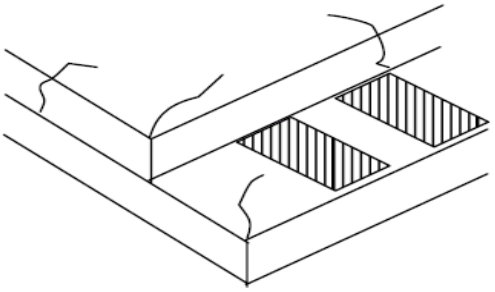
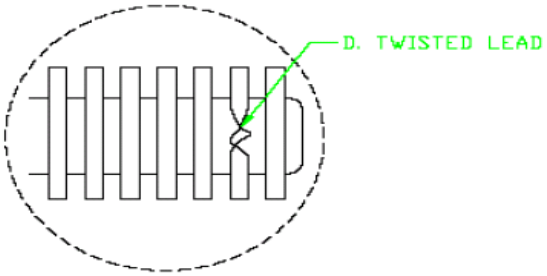
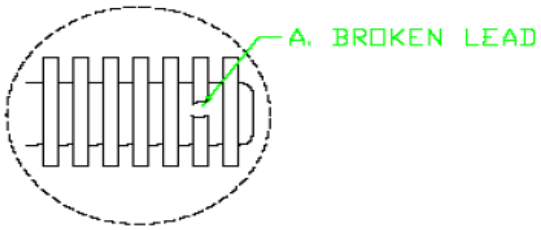
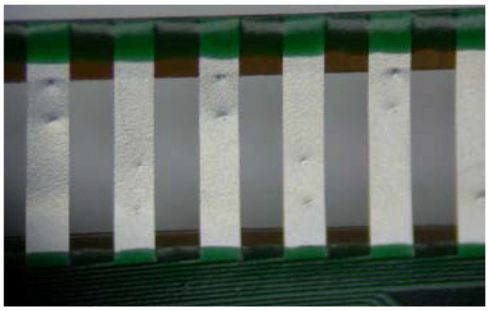
Temperature:	23±5℃
Humidity:	55±15%RH
Fluorescent lamp:	30 W
Distance between the Panel & Eyes of the Inspector:	≧30cm
Distance between the Panel & the lamp:	≧50cm

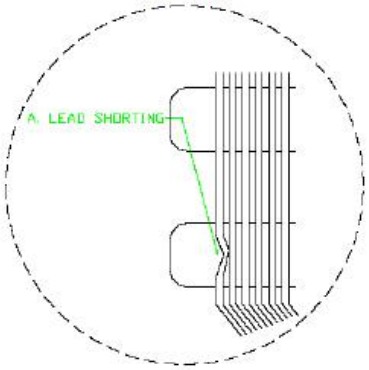
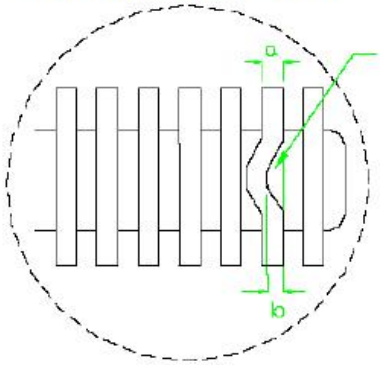
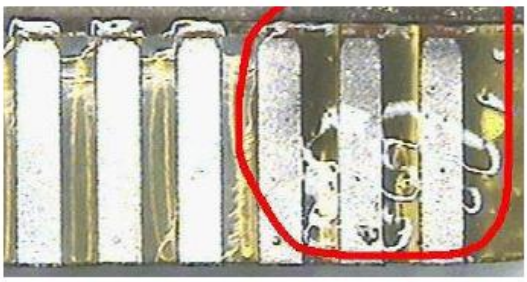
Finger glove (or finger cover) must be worn by the inspector.
Inspection table or jig must be anti-electrostatic

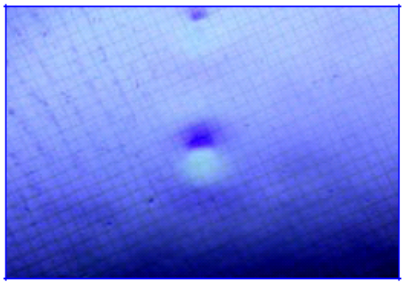
7.2.4 Standard of appearance inspection

Partition	AQL	Definition
Major	0.65	Defects in Pattern Check (Display On)
Minor	1.0	Defects in Cosmetic Check (Display Off)

Check Item	Classification	Criteria
Panel General Chipping	Minor	X > 6 mm (Along with Edge) Y > 1 mm (Perpendicular to edge) 

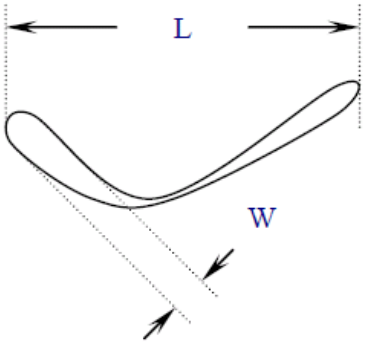
Check Item	Classification	Criteria
Panel Crack	Minor	Any crack is not allowable. 
Cupper Exposed (Even Pin or Film)	Minor	Not Allowable by Naked Eye Inspection
Film or Trace Damage	Minor	
Terminal Lead Twist	Minor	Not Allowable 
Terminal Lead Broken	Minor	Not Allowable 
Terminal Lead Prober Mark	Acceptable	

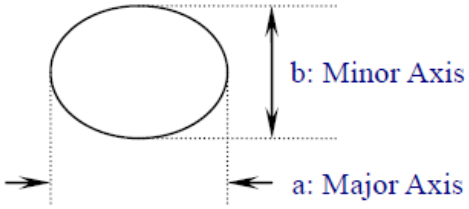
<table>
<tr><th>Check Item</th><th>Classification</th><th>Criteria</th></tr>
<tr><td rowspan="2">Terminal Lead Bent
(Not Twist or Broken)</td><td>Minor</td><td>NG if any bent lead cause lead shorting.
 
</td></tr>
<tr><td>Minor</td><td>NG for horizontally bent lead more than 50% of its width.
 
</td></tr>
<tr><td>Glue or Contamination on Pin
(Couldn’t Be Removed by Alcohol)</td><td>Minor</td><td>  </td></tr>
<tr><td>Ink Marking on Back Side of panel
(Exclude on Film)</td><td>Acceptable</td><td>Ignore for Any</td></tr>
</table>

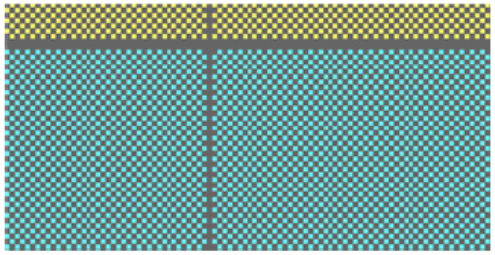
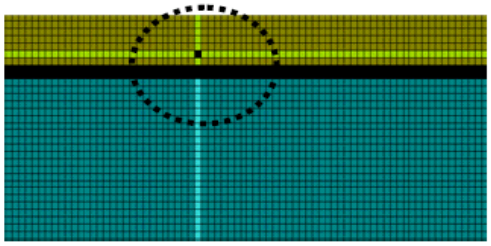
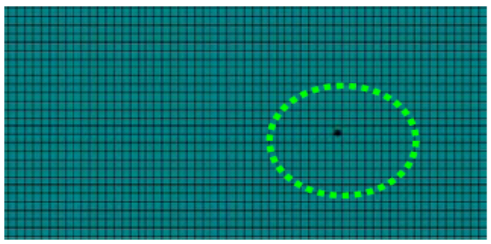
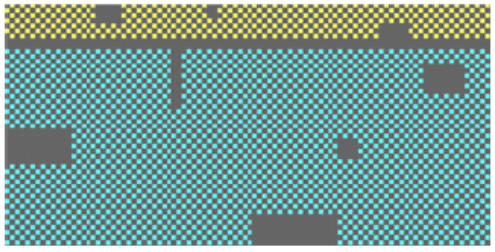
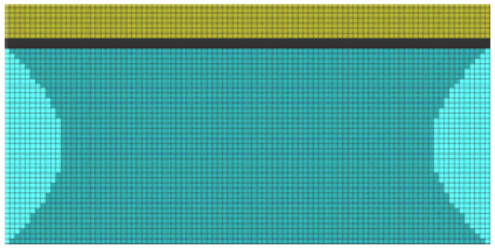
Check Item	Classification	Criteria
Any Dirt & Scratch on Polarizer's Protective Film	Acceptable	Ignore for not Affect the Polarizer
Scratches, Fiber, Line-Shape Defect (On Polarizer)	Minor	$W \le 0.1$ Ignore $W > 0.1, L \le 2$ $n \le 1$ $L > 2$ $n = 0$
Dirt, Black Spot, Foreign Material, (On Polarizer)	Minor	$\Phi \le 0.1$ Ignore $0.1 < \Phi \le 0.25$ $n \le 1$ $0.25 < \Phi$ $n = 0$
Dent, Bubbles, White spot (Any Transparent Spot on Polarizer)	Minor	$\Phi \le 0.5$ ➔ Ignore if no Influence on Display $0.5 < \Phi$ $n = 0$ 
Fingerprint, Flow Mark (On Polarizer)	Minor	Not Allowable

* Protective film should not be tear off when cosmetic check.

** Definition of W & L & Φ (Unit: mm): $\Phi = (a + b) / 2$





Check Item	Classification	Criteria
No Display	Major	
Flicker	Major	Not Allowable
Missing Line	Major	
Pixel Short	Major	
Darker Pixel	Major	
Wrong Display	Major	
Un-uniform	Major	

7.3 DEALING WITH CUSTOMER COMPLAINTS

7.3.1 Non-conforming analysis

Purchaser should supply Densitron with detailed data of non-conforming sample.
After accepting it, Densitron should complete the analysis in two weeks from receiving the sample.
If the analysis cannot be completed on time, Densitron must inform the purchaser.

7.3.2 Handling of non-conforming displays

If any non-conforming displays are found during customer acceptance inspection which Densitron is clearly responsible for, return them to Densitron.
Both Densitron and customer should analyse the reason and discuss the handling of non-conforming displays when the reason is not clear.
Equally, both sides should discuss and come to agreement for issues pertaining to modification of Densitron quality assurance standard.

8 RELIABILITY SPECIFICATION

8.1 RELIABILITY TESTS

Test Item	Test Condition	Evaluation and assessment
High Temperature Operation	70°C±2,120 hours	No abnormalities in function and appearance
Low Temperature Operation	-40°C±2, 120 hours	No abnormalities in function and appearance
High Temperature Storage	85°C±2, 1220 hours	No abnormalities in function and appearance
Low Temperature Storage	-40°C±2, 120 hours	No abnormalities in function and appearance
High Temperature & High Humidity Storage(Operation)	60°C±2, 90%RH, 120 hours	No abnormalities in function and appearance
Thermal Shock	24 cycle of -40°C 1 Hour, R.T. 5 min, 85°C 1 Hour	No abnormalities in function and appearance

- The samples used for above tests do not include polarizer.
- No moisture condensation is observed during tests.

8.1.1 FAILURE CHECK STANDARD

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure teat at 23±5 °C ; 55±15% RH

8.2 LIFE TIME

Item	Description
1	Function, performance, appearance, etc. shall be free from remarkable deterioration more than 10,000 hours under ordinary operating conditions of room temperature (25±10 °C), normal humidity (45±20% RH), and in area not exposed to direct sunlight.
2	End of lifetime is specified as 50% of initial brightness.

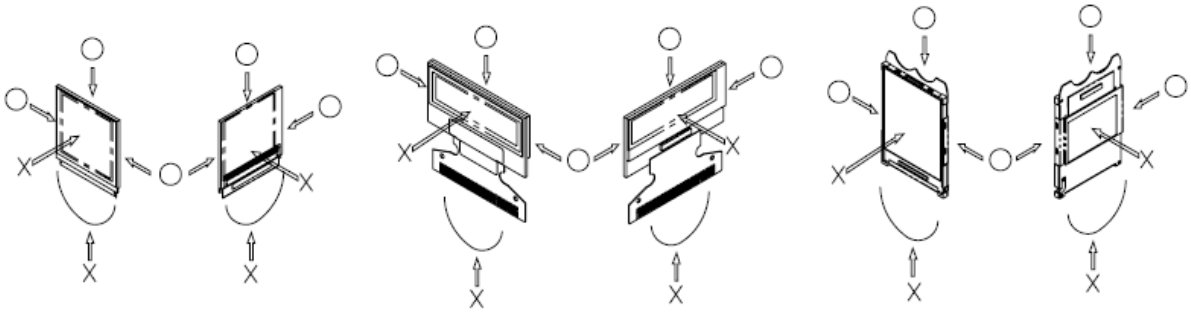
8.3 FAILURE CHECK STANDARD

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5°C; 55±15% RH.

9 HANDLING PRECAUTIONS

9.1 HANDLING PRECAUTIONS

1) Since the display panel is being made of glass, do not apply mechanical impacts such us dropping from a high position.
2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.
3) If pressure is applied to the display surface or its neighborhood of the OEL display module, the cell structure may be damaged and be careful not to apply pressure to these sections.
4) The polarizer covering the surface of the OEL display module is soft and easily scratched. Please be careful when handling the OEL display module.
5) When the surface of the polarizer of the OEL display module has soil, clean the surface. It takes advantage of by using following adhesion tape.
   * Scotch Mending Tape No. 810 or an equivalent
   Never try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy.
   Also, pay attention that the following liquid and solvent may spoil the polarizer:
   * Water
   * Ketone
   * Aromatic Solvents
6) Hold OEL display module very carefully when placing OEL display module into the system housing. Do not apply excessive stress or pressure to OEL display module. And, do not over bend the film with electrode pattern layouts. These stresses will influence the display performance. Also, secure sufficient rigidity for the outer cases.



7) Do not apply stress to the LSI chips and the surrounding molded sections.
8) Do not disassemble nor modify the OEL display module.
9) Do not apply input signals while the logic power is off.
10) Pay sufficient attention to the working environments when handing OEL display modules to prevent occurrence of element breakage accidents by static electricity.
    * Be sure to make human body grounding when handling OEL display modules.
    * Be sure to ground tools to use or assembly such as soldering irons.
    * To suppress generation of static electricity, avoid carrying out assembly work under dry environments.

* Protective film is being applied to the surface of the display panel of the OEL display module. Be careful since static electricity may be generated when exfoliating the protective film.

11) Protection film is being applied to the surface of the display panel and removes the protection film before assembling it. At this time, if the OEL display module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).
12) If electric current is applied when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

9.2 STORAGE PRECAUTIONS

1) When storing OEL display modules, put them in static electricity preventive bags avoiding exposure to direct sun light nor to lights of fluorescent lamps, etc. and, also, avoiding high temperature and high humidity environments or low temperature (less than 0°C) environments. (We recommend you to store these modules in the packaged state when they were shipped from Densitron Technologies Plc.) At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.
2) If electric current is applied when water drops are adhering to the surface of the OEL display module, when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

9.3 DESIGNING PRECAUTIONS

1) The absolute maximum ratings are the ratings which cannot be exceeded for OEL display module, and if these values are exceeded, panel damage may be happen.
2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the VIL and VIH specifications and, at the same time, to make the signal line cable as short as possible.
3) We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (VDD). (Recommend value: 0.5A)
4) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighboring devices.
5) As for EMI, take necessary measures on the equipment side basically.
6) When fastening the OEL display module, fasten the external plastic housing section.
7) If power supply to the OEL display module is forcibly shut down by such errors as taking out the main battery while the OEL display panel is in operation, we cannot guarantee the quality of this OEL display module.
8) The electric potential to be connected to the rear face of the IC chip should be as follows: US2066

* Connection (contact) to any other potential than the above may lead to rupture of the IC.

9.4 OTHER PRECAUTIONS

1) When an OEL display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur. Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored. Also, there will be no problem in the reliability of the module.
2) To protect OEL display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the OEL display modules.
   * Pins and electrodes
   * Pattern layouts such as the FPC
3) With this OEL display module, the OEL driver is being exposed. Generally speaking, semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if this OEL driver is exposed to light, malfunctioning may occur.
   * Design the product and installation method so that the OEL driver may be shielded from light in actual usage.
   * Design the product and installation method so that the OEL driver may be shielded from light during the inspection processes.
4) Although this OEL display module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed. It therefore is necessary to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.
5) We recommend you to construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.

9.5 PRECAUTIONS WHEN DISPOSING OF THE OEL DISPLAY MODULES

1) Request the qualified companies to handle industrial wastes when disposing of the OEL display modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.

10 SUPPORTED ACCESSORIES

10.1 DUO KIT

Densitron has developed an easy to use yet powerful development and demonstration tool for driving its range of Passive Matrix OLED displays from the USB port of a PC.
DUO (Densitron USB OLED) kit is hot pluggable and does not require extra cables or power supply to run, allowing users to be up and running in minutes.

The kit consists of an OLED display with transition Board, USB controller card, mini USB cable and a CD with software application and drivers.

Part number: UNDER DEVELOPMENT

10.2 TRANSITION BOARD CARD

A Transition board card is like a daughterboard which is meant to be a circuit board for connections between the baseboards (DUO).
It has connector pins for interfacing between the display and the baseboards.
It also includes the OLED display.
Part number: PDT-N-9639BE-4A

10.3 CONNECTOR BOARD CARD

A Connector board card is also a daughterboard which is a circuit board for connection between a microprocessor or microcontroller (customer's system).
Part number: EVK-CONNECT-031

10.4 CONNECTOR

Type: hot bar soldering process
No. of connections: 28
Pitch: 0.65mm