FM18W08

256Kb Wide Voltage Bytewide F-RAM

Features

256Kbit Ferroelectric Nonvolatile RAM

- Organized as 32,768 x 8 bits
- High Endurance 100 Trillion (10^{14}) Read/Writes
- 38 year Data Retention
- NoDelay™ Writes
- Advanced High-Reliability Ferroelectric Process

Superior to BBSRAM Modules

- No Battery Concerns
- Monolithic Reliability
- True Surface Mount Solution, No Rework Steps
- Superior for Moisture, Shock, and Vibration
- Resistant to Negative Voltage Undershoots

SRAM & EEPROM Compatible

- JEDEC 32Kx8 SRAM & EEPROM pinout
- 70 ns Access Time
- 130 ns Cycle Time

Low Power Operation

- Wide Voltage Operation 2.7V to 5.5V
- 12 mA Active Current
- 20 µA (typ.) Standby Current

Industry Standard Configuration

- Industrial Temperature -40° C to +85° C
- 28-pin "Green"/RoHS SOIC Package

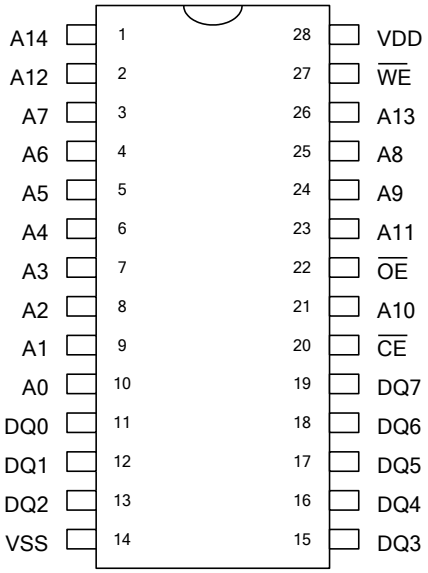
Description

The FM18W08 is a 256-kilobit nonvolatile memory employing an advanced ferroelectric process. A ferroelectric random access memory or F-RAM is nonvolatile but operates in other respects as a RAM. It provides data retention for 38 years while eliminating the reliability concerns, functional disadvantages and system design complexities of battery-backed SRAM (BBSRAM). Fast write timing and high write endurance make F-RAM superior to other types of nonvolatile memory.

In-system operation of the FM18W08 is very similar to other RAM devices. Minimum read- and write-cycle times are equal. The F-RAM memory, however, is nonvolatile due to its unique ferroelectric memory process. Unlike BBSRAM, the FM18W08 is a truly monolithic nonvolatile memory. It provides the same functional benefits of a fast write without the disadvantages associated with modules and batteries or hybrid memory solutions.

These capabilities make the FM18W08 ideal for nonvolatile memory applications requiring frequent or rapid writes in a bytewide environment. The availability of a true surface-mount package improves the manufacturability of new designs. Device specifications are guaranteed over an industrial temperature range of -40°C to +85°C.

Pin Configuration



Ordering Information	
FM18W08-SG	28-pin "Green" SOIC

This is a product in the pre-production phase of development. Device characterization is complete and Ramtron does not expect to change the specifications. Ramtron will issue a Product Change Notice if any specification changes are made.

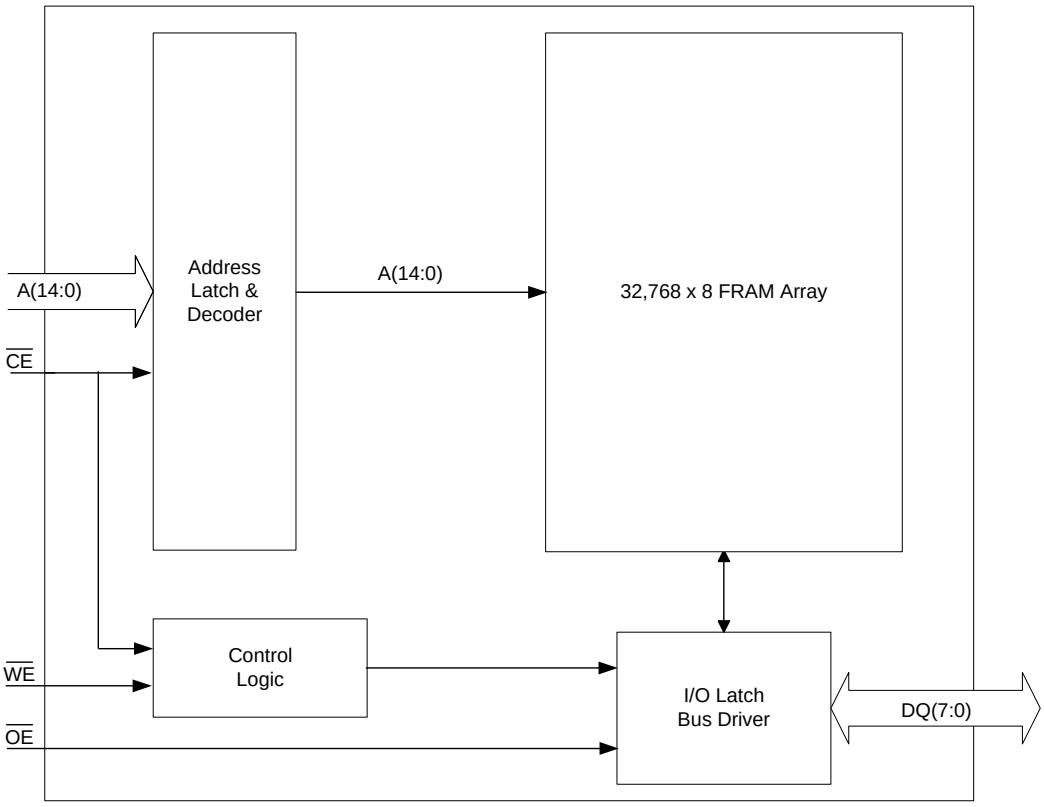


Figure 1. Block Diagram

Pin Description

Pin Name	Type	Description
A(14:0)	Input	Address: The 15 address lines select one of 32,768 bytes in the F-RAM array. The address value is latched on the falling edge of /CE.
DQ(7:0)	I/O	Data: 8-bit bi-directional data bus for accessing the F-RAM array.
/CE	Input	Chip Enable: /CE selects the device when low. Asserting /CE low causes the address to be latched internally. Address changes that occur after /CE goes low will be ignored until the next falling edge occurs.
/OE	Input	Output Enable: Asserting /OE low causes the FM18W08 to drive the data bus when valid data is available. Deasserting /OE high causes the DQ pins to be tri-stated.
/WE	Input	Write Enable: Asserting /WE low causes the FM18W08 to write the contents of the data bus to the address location latched by the falling edge of /CE.
VDD	Supply	Supply Voltage
VSS	Supply	Ground

Functional Truth Table

/CE	/WE	Function
H	X	Standby/Precharge
↓	X	Latch Address (and Begin Write if /WE=low)
L	H	Read
L	↓	Write

Note: The /OE pin controls only the DQ output buffers.

Overview

The FM18W08 is a bytewide F-RAM memory. The memory array is logically organized as 32,768 x 8 and is accessed using an industry standard parallel interface. All data written to the part is immediately nonvolatile with no delay. Functional operation of the F-RAM memory is the same as SRAM type devices, except the FM18W08 requires a falling edge of /CE to start each memory cycle.

Memory Architecture

Users access 32,768 memory locations each with 8 data bits through a parallel interface. The complete 15-bit address specifies each of the 32,768 bytes uniquely. Internally, the memory array is organized into 4092 rows of 8-bytes each. This block segmentation has no effect on operation, however the user may wish to group data into blocks by its endurance characteristics as explained on page 4.

The cycle time is the same for read and write memory operations. This simplifies memory controller logic and timing circuits. Likewise the access time is the same for read and write memory operations. When /CE is deasserted high, a precharge operation begins, and is required of every memory cycle. Thus unlike SRAM, the access and cycle times are not equal. Writes occur immediately at the end of the access with no delay. Unlike an EEPROM, it is not necessary to poll the device for a ready condition since writes occur at bus speed.

It is the user's responsibility to ensure that V_{DD} remains within datasheet tolerances to prevent incorrect operation. Also proper voltage level and timing relationships between V_{DD} and /CE must be maintained during power-up and power-down events. See Power Cycle Timing diagram on page 9.

Memory Operation

The FM18W08 is designed to operate in a manner similar to other bytewide memory products. For users familiar with BBSRAM, the performance is comparable but the bytewide interface operates in a slightly different manner as described below. For users familiar with EEPROM, the obvious differences result from the higher write performance of F-RAM technology including NoDelay writes and much higher write endurance.

Read Operation

A read operation begins on the falling edge of /CE. At this time, the address bits are latched and a memory cycle is initiated. Once started, a full memory cycle must be completed internally even if /CE goes inactive. Data becomes available on the bus after the access time has been satisfied.

After the address has been latched, the address value may be changed upon satisfying the hold time parameter. Unlike an SRAM, changing address values will have no effect on the memory operation after the address is latched.

The FM18W08 will drive the data bus when /OE is asserted low. If /OE is asserted after the memory access time has been satisfied, the data bus will be driven with valid data. If /OE is asserted prior to completion of the memory access, the data bus will not be driven until valid data is available. This feature minimizes supply current in the system by eliminating transients caused by invalid data being driven onto the bus. When /OE is inactive the data bus will remain tri-stated.

Write Operation

Writes occur in the FM18W08 in the same time interval as reads. The FM18W08 supports both /CE- and /WE-controlled write cycles. In all cases, the address is latched on the falling edge of /CE.

In a /CE controlled write, the /WE signal is asserted prior to beginning the memory cycle. That is, /WE is low when /CE falls. In this case, the part begins the memory cycle as a write. The FM18W08 will not drive the data bus regardless of the state of /OE.

In a /WE controlled write, the memory cycle begins on the falling edge of /CE. The /WE signal falls after the falling edge of /CE. Therefore, the memory cycle begins as a read. The data bus will be driven according to the state of /OE until /WE falls. The timing of both /CE- and /WE-controlled write cycles is shown in the electrical specifications.

Write access to the array begins asynchronously after the memory cycle is initiated. The write access terminates on the rising edge of /WE or /CE, whichever is first. Data set-up time, as shown in the electrical specifications, indicates the interval during which data cannot change prior to the end of the write access.

Unlike other truly nonvolatile memory technologies, there is no write delay with F-RAM. Since the read and write access times of the underlying memory are the same, the user experiences no delay through the bus. The entire memory operation occurs in a single bus cycle. Therefore, any operation including read or write can occur immediately following a write. Data polling, a technique used with EEPROMs to determine if a write is complete, is unnecessary.

Precharge Operation

The precharge operation is an internal condition that prepares the memory for a new access. All memory cycles consist of a memory access and a precharge. The precharge is initiated by deasserting the /CE pin high. It must remain high for at least the minimum precharge time t_{PC}.

The user determines the beginning of this operation since a precharge will not begin until /CE rises. However, the device has a maximum /CE low time specification that must be satisfied.

Endurance

Internally, a F-RAM operates with a read and restore mechanism. Therefore, each read and write cycle involves a change of state. The memory architecture is based on an array of rows and columns. Each read or write access causes an endurance cycle for an entire row. In the FM18W08, a row is 64 bits wide. Every 8-byte boundary marks the beginning of a new row. Endurance can be optimized by ensuring frequently accessed data is located in different rows. Regardless, F-RAM offers substantially higher write endurance than other nonvolatile memories. The rated endurance limit of 10^{14} cycles will allow 150,000 accesses per second to the same row for over 20 years.

F-RAM Design Considerations

When designing with F-RAM for the first time, users of SRAM will recognize a few minor differences. First, bytewide F-RAM memories latch each address on the falling edge of chip enable. This allows the address bus to change after starting the memory access. Since every access latches the memory address on the falling edge of /CE, users cannot ground it as they might with SRAM.

Users who are modifying existing designs to use F-RAM should examine the memory controller for timing compatibility of address and control pins. Each memory access must be qualified with a low transition of /CE. In many cases, this is the only change required. An example of the signal relationships is shown in Figure 2 below. Also shown is a common SRAM signal relationship that will not work for the FM18W08.

The reason for /CE to strobe for each address is two-fold: it latches the new address and creates the necessary precharge period while /CE is high.

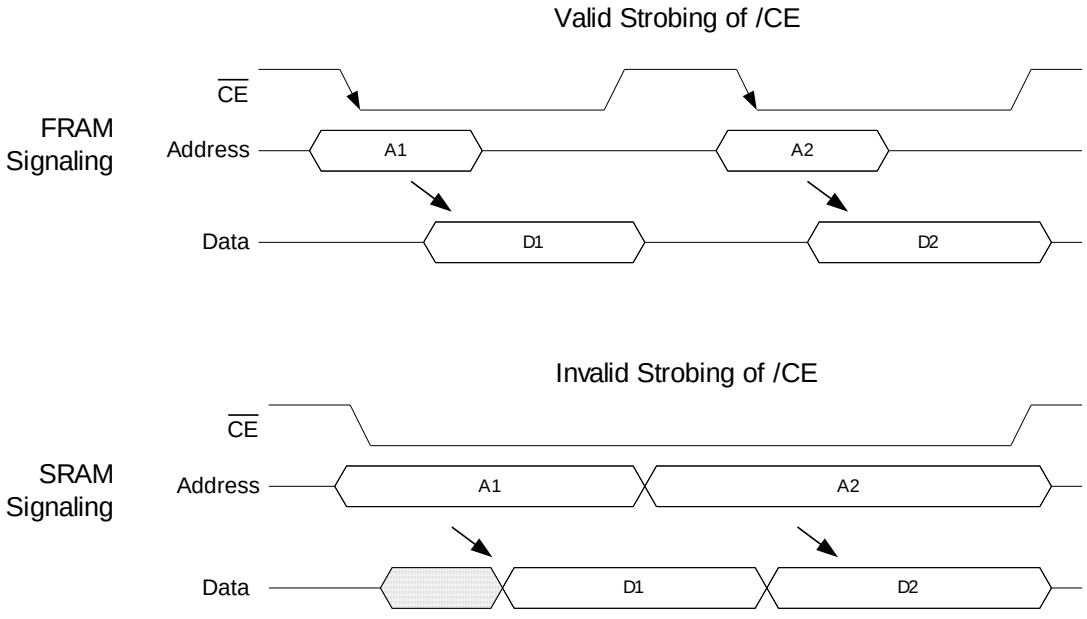


Figure 2. Chip Enable and Memory Address Relationships

A second design consideration relates to the level of V_{DD} during operation. Battery-backed SRAMs are forced to monitor V_{DD} in order to switch to battery backup. They typically block user access below a certain V_{DD} level in order to prevent loading the battery with current demand from an active SRAM. The user can be abruptly cut off from access to the nonvolatile memory in a power down situation with no warning or indication.

F-RAM memories do not need this system overhead. The memory will not block access at any V_{DD} level that complies with the specified operating range. The user should take measures to prevent the processor from accessing memory when V_{DD} is out-of-tolerance. The common design practice of holding a processor in reset during powerdown may be sufficient. It is recommended that Chip Enable is pulled high and allowed to track V_{DD} during powerup and powerdown cycles. It is the user's responsibility to ensure that chip enable is high to prevent accesses below V_{DD} min. (2.7V). Figure 3 shows a pullup resistor on /CE which will keep the pin high during power cycles assuming the MCU/MPU pin tri-states during the reset condition. The pullup resistor value should be chosen to ensure the /CE pin tracks V_{DD} yet a high enough value that the current drawn when /CE is low is not an issue.

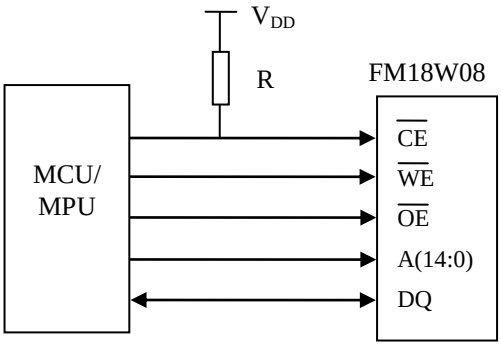


Figure 3. Use of Pullup Resistor on /CE

Electrical Specifications

Absolute Maximum Ratings

Symbol	Description	Ratings
V_{DD}	Power Supply Voltage with respect to V_{SS}	-1.0V to +7.0V
V_{IN}	Voltage on any pin with respect to V_{SS}	-1.0V to +7.0V and $V_{IN} < V_{DD}+1.0V$
T_{STG}	Storage Temperature	-55°C to + 125°C
T_{LEAD}	Lead Temperature (Soldering, 10 seconds)	260° C
V_{ESD}	Electrostatic Discharge Voltage - Human Body Model (AEC-Q100-002 Rev. E) - Charged Device Model (AEC-Q100-011 Rev. B) - Machine Model (AEC-Q100-003 Rev. E)	 4kV 1.25kV 300V
	Package Moisture Sensitivity Level	MSL-2

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and the functional operation of the device at these or any other conditions above those listed in the operational section of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

DC Operating Conditions (T_A = -40° C to + 85° C, V_{DD} = 2.7V to 5.5V unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{DD}	Power Supply	2.7	3.3	5.5	V	
I_{DD}	V_{DD} Supply Current		-	12	mA	1
I_{SB}	Standby Current		20	50	µA	2
I_{LI}	Input Leakage Current	-		±1	µA	3
I_{LO}	Output Leakage Current	-		±1	µA	3
V_{IH}	Input High Voltage	$0.7*V_{DD}$		$V_{DD}+0.3$	V	
V_{IL}	Input Low Voltage	-0.3		$0.3*V_{DD}$	V	
V_{OH1}	Output High Voltage (I_{OH} = -1 mA, V_{DD}=2.7V)	2.4			V	
V_{OH2}	Output High Voltage (I_{OH} = -100 µA)	V_{DD}-0.2			V	
V_{OL1}	Output Low Voltage (I_{OL} = 2 mA, V_{DD}=2.7V)			0.4	V	
V_{OL2}	Output Low Voltage (I_{OL} = 150 µA)			0.2	V	

Notes

1. V_{DD} = 5.5V, /CE cycling at minimum cycle time. All inputs at CMOS levels, all outputs unloaded.
2. /CE at V_{IH}, All other pins at CMOS levels (0.2V or V_{DD}-0.2V).
3. V_{IN}, V_{OUT} between V_{DD} and V_{SS}.

Read Cycle AC Parameters (T_A = -40°C to + 85°C, C_L = 30 pF, unless otherwise specified)

Symbol	Parameter	V_{DD} 2.7 to 3.0V		V_{DD} 3.0 to 5.5V		Units	Notes
		Min	Max	Min	Max		
t_{CE}	Chip Enable Access Time (to data valid)		80		70	ns	
t_{CA}	Chip Enable Active Time	80		70		ns	
t_{RC}	Read Cycle Time	145		130		ns	
t_{PC}	Precharge Time	65		60		ns	
t_{AS}	Address Setup Time	0		0		ns	
t_{AH}	Address Hold Time	15		15		ns	
t_{OE}	Output Enable Access Time		15		12	ns	
t_{HZ}	Chip Enable to Output High-Z		15		15	ns	1
t_{OHZ}	Output Enable to Output High-Z		15		15	ns	1

Write Cycle AC Parameters (T_A = -40°C to + 85°C, unless otherwise specified)

Symbol	Parameter	V_{DD} 2.7 to 3.0V		V_{DD} 3.0 to 5.5V		Units	Notes
		Min	Max	Min	Max		
t_{CA}	Chip Enable Active Time	80		70		ns	
t_{CW}	Chip Enable to Write High	80		70		ns	
t_{WC}	Write Cycle Time	145		130		ns	
t_{PC}	Precharge Time	65		60		ns	
t_{AS}	Address Setup Time	0		0		ns	
t_{AH}	Address Hold Time	15		15		ns	
t_{WP}	Write Enable Pulse Width	50		40		ns	
t_{DS}	Data Setup	40		30		ns	
t_{DH}	Data Hold	0		0		ns	
t_{WZ}	Write Enable Low to Output High Z		15		15	ns	1
t_{WX}	Write Enable High to Output Driven	10		10		ns	1
t_{HZ}	Chip Enable to Output High-Z		15		15	ns	1
t_{WS}	Write Enable Setup	0		0		ns	2
t_{WH}	Write Enable Hold	0		0		ns	2

Notes

1 This parameter is periodically sampled and not 100% tested.

2 The relationship between /CE and /WE determines if a /CE- or /WE-controlled write occurs. There is no timing specification associated with this relationship.

Data Retention

Symbol	Parameter	Min	Max	Units	Notes
T_{DR}	@ +85ºC	10	-	Years	
	@ +80ºC	19	-	Years	
	@ +75ºC	38	-	Years	

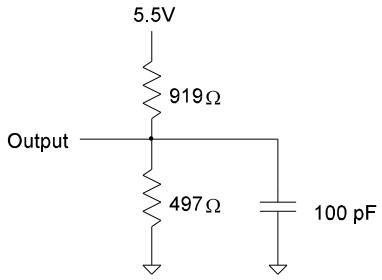
Capacitance (T_A = 25° C, f=1.0 MHz, V_{DD} = 5V)

Symbol	Parameter	Min	Max	Units	Notes
$C_{I/O}$	Input/Output Capacitance (DQ)	-	8	pF	
C_{IN}	Input Capacitance	-	6	pF	

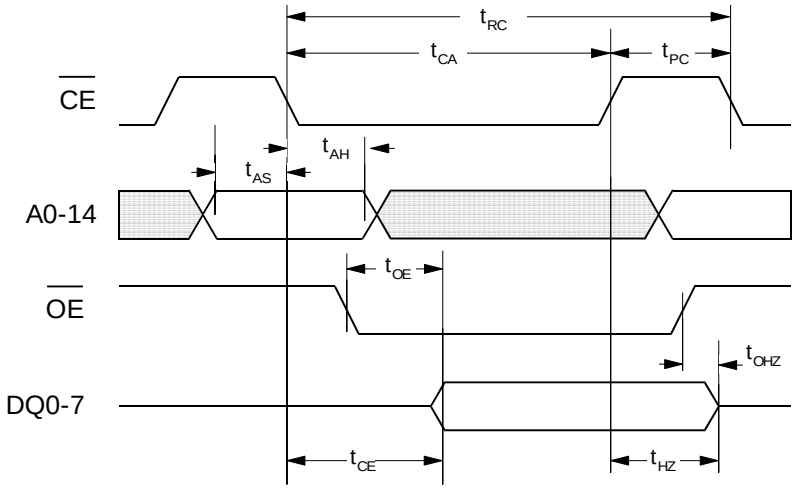
AC Test Conditions

Input Pulse Levels	10% and 90% of V_{DD}
Input rise and fall times	5 ns
Input and output timing levels	0.5 V_{DD}

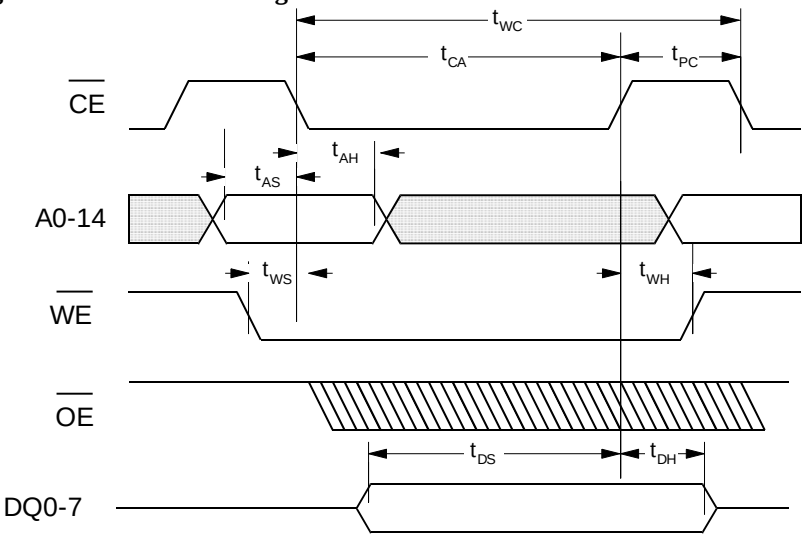
Equivalent AC Load Circuit



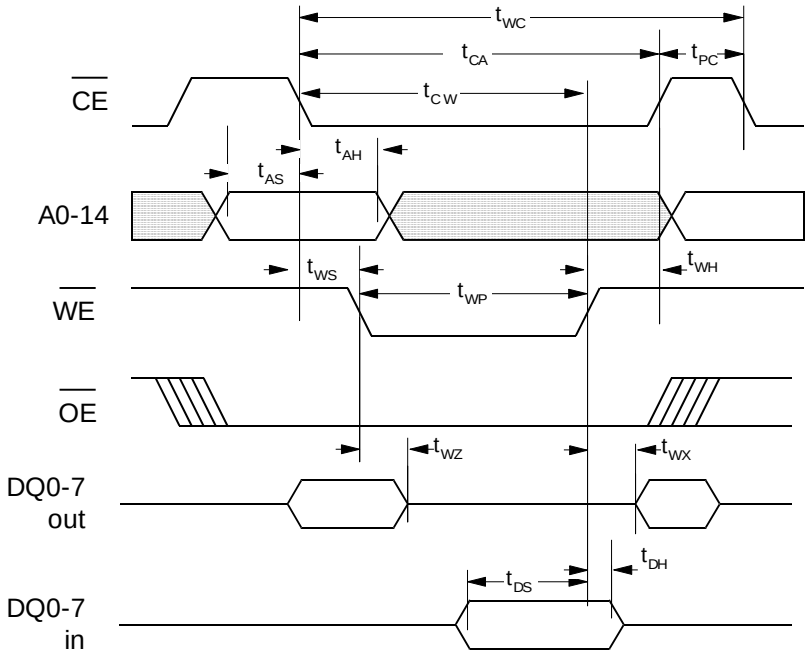
Read Cycle Timing



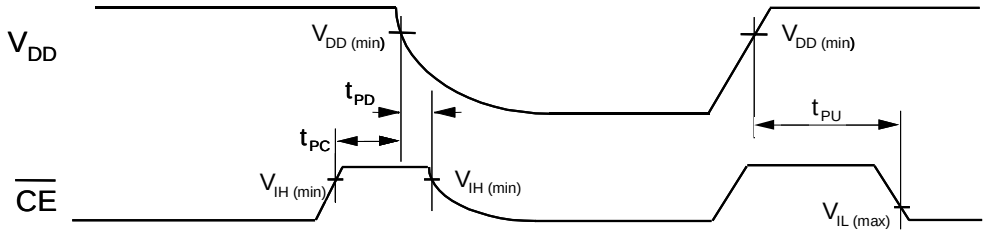
Write Cycle Timing - /CE Controlled Timing



Write Cycle Timing - /WE Controlled Timing



Power Cycle Timing



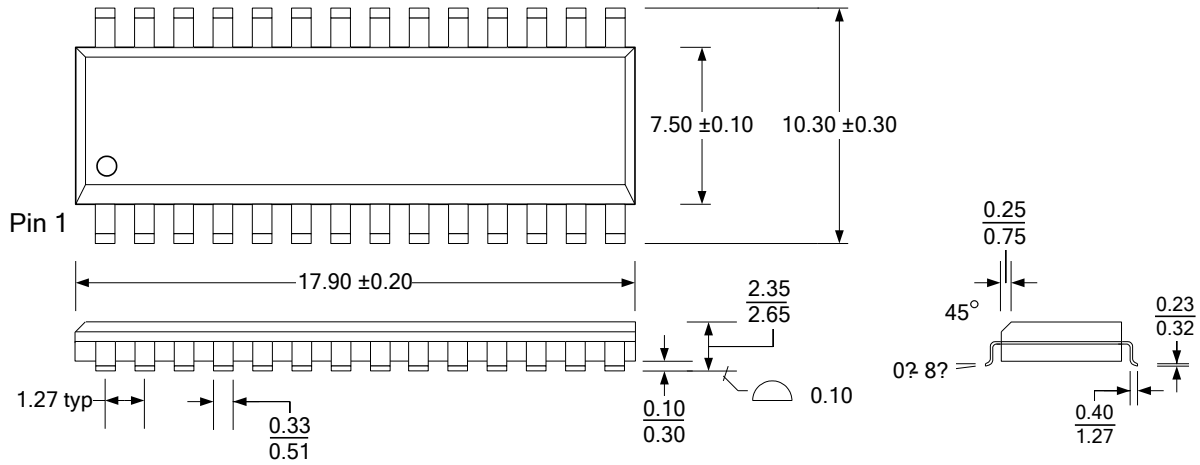
Power Cycle Timing (T_A = -40°C to + 85°C, V_{DD} = 2.7V to 5.5V unless otherwise specified)

Symbol	Parameter	Min	Max	Units	Notes
t_{PU}	V_{DD}(min) to First Access Start	10	-	ms	
t_{PD}	Last Access Complete to V_{DD}(min)	0	-	µs	
t_{VR}	V_{DD} Rise Time	30	-	µs/V	1
t_{VF}	V_{DD} Fall Time	30	-	µs/V	1

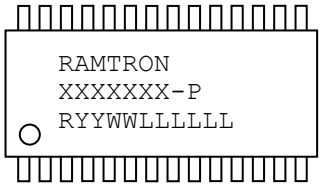
Notes

1. Slope measured at any point on V_{DD} waveform.

28-pin SOIC (JEDEC MS-013 variation AE)
All dimensions in millimeters



SOIC Package Marking Scheme



Legend:
XXXXXX= part number, P= package type (-SG)
R=rev code, YY=year, WW=work week, LLLLLL= lot code

Example: FM18W08, 70ns speed, "Green"/RoHS SOIC package,
A die rev., Year 2010, Work Week 37, Lot code 00002G

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RAMTRON
FM18W08-SG
A103700002G
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Revision History

Revision	Date	Summary
1.0	11/22/2010	Initial Release
1.1	12/20/2010	Updated MSL rating.
1.2	3/10/2011	Changed t_{PU} and t_{VF} spec limits.
2.0	12/20/2011	Changed to Pre-Production status.
2.1	1/6/2012	Changed t_{VF} spec.

Document History

Document Title: FM18W08 256Kb Wide Voltage Bytewide F-RAM
Document Number: 001-86207

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	3912933	GVCH	02/25/2013	New Spec

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