

# 74HC573; 74HCT573

Octal D-type transparent latch; 3-state

Rev. 7 — 4 March 2016

Product data sheet

## 1. General description

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The 74HC573; 74HCT573 is an 8-bit D-type transparent latch with 3-state outputs. The device features latch enable (LE) and output enable ( $\overline{OE}$ ) inputs. When LE is HIGH, data at the inputs enter the latches. In this condition the latches are transparent, a latch output will change each time its corresponding D-input changes. When LE is LOW the latches store the information that was present at the inputs a set-up time preceding the HIGH-to-LOW transition of LE. A HIGH on  $\overline{OE}$  causes the outputs to assume a high-impedance OFF-state. Operation of the  $\overline{OE}$  input does not affect the state of the latches. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of  $V_{CC}$ .

## 2. Features and benefits

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- Input levels:
  - ◆ For 74HC573: CMOS level
  - ◆ For 74HCT573: TTL level
- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors and microcomputers
- 3-state non-inverting outputs for bus-oriented applications
- Common 3-state output enable input
- Multiple package options
- Complies with JEDEC standard no. 7 A
- ESD protection:
  - ◆ HBM JESD22-A114F exceeds 2 000 V
  - ◆ MM JESD22-A115-A exceeds 200 V
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$  and from  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$

### 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74HC573D	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74HCT573D				
74HC573DB	-40 °C to +125 °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1
74HCT573DB				
74HC573PW	-40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74HCT573PW				
74HC573BQ	-40 °C to +125 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1
74HCT573BQ				

### 4. Functional diagram

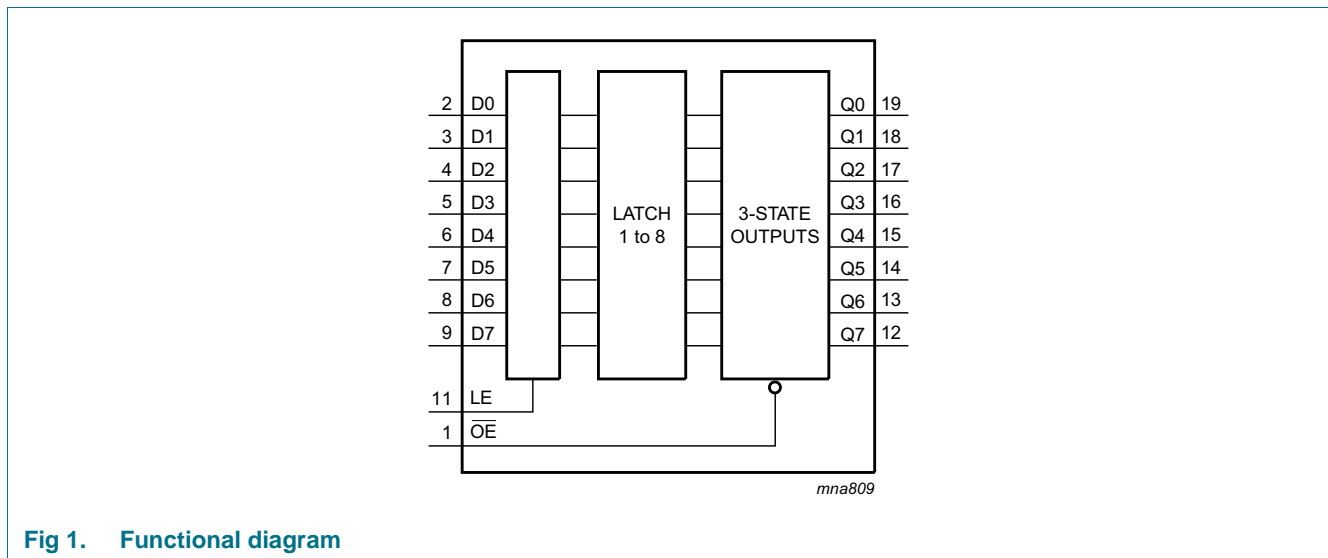


Fig 1. Functional diagram

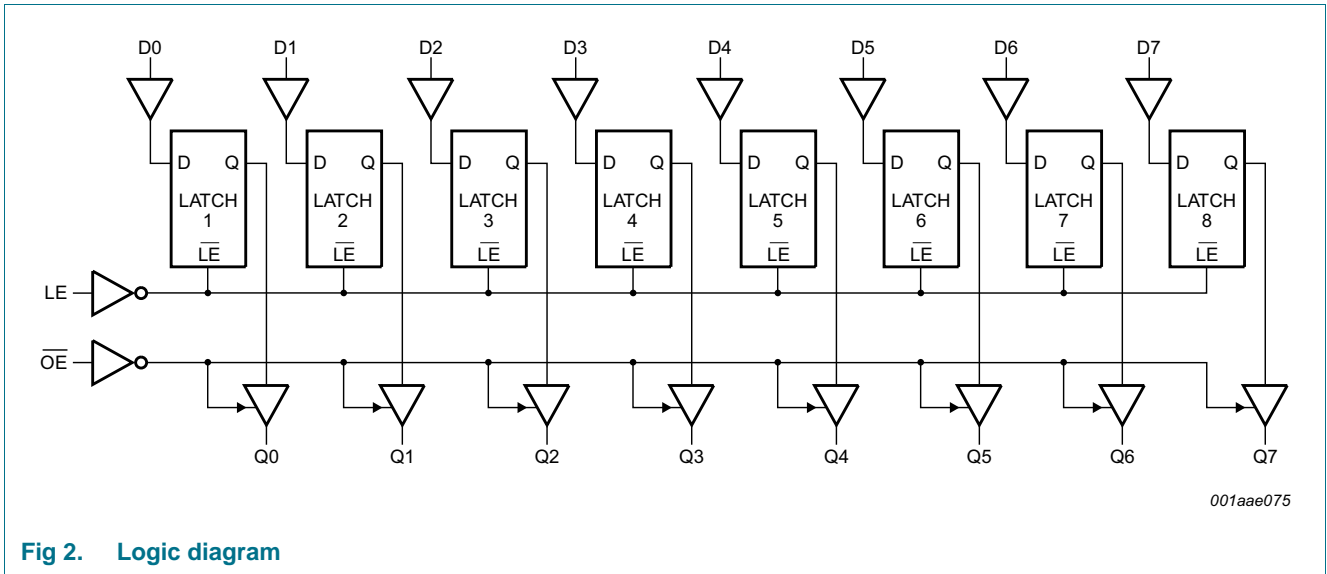


Fig 2. Logic diagram

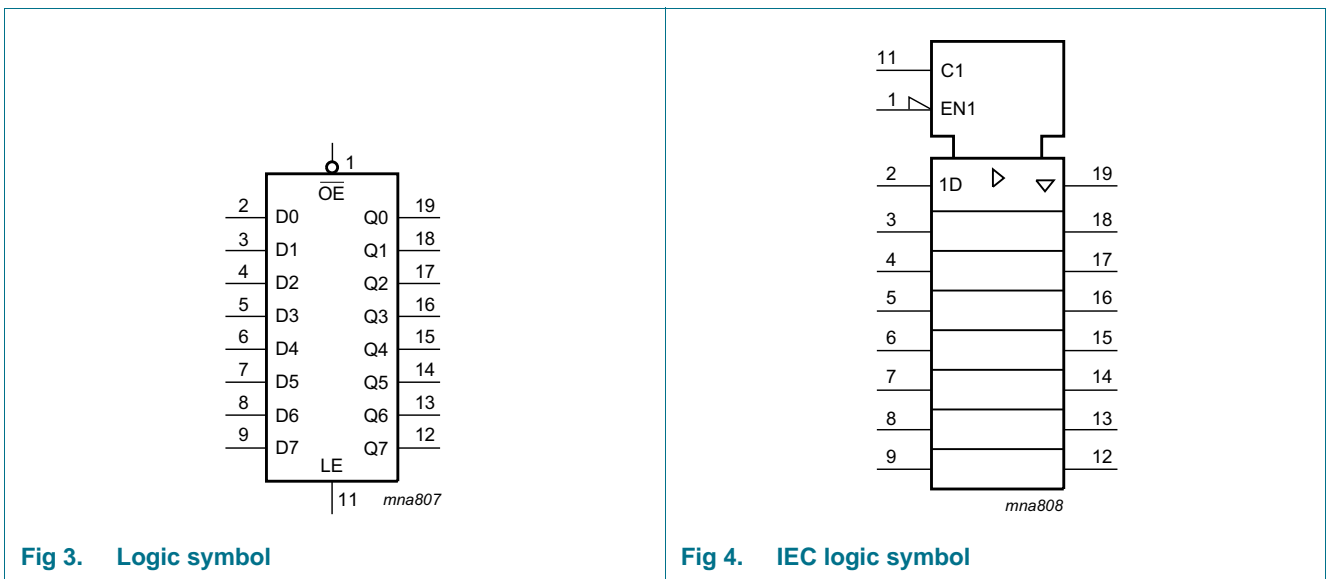
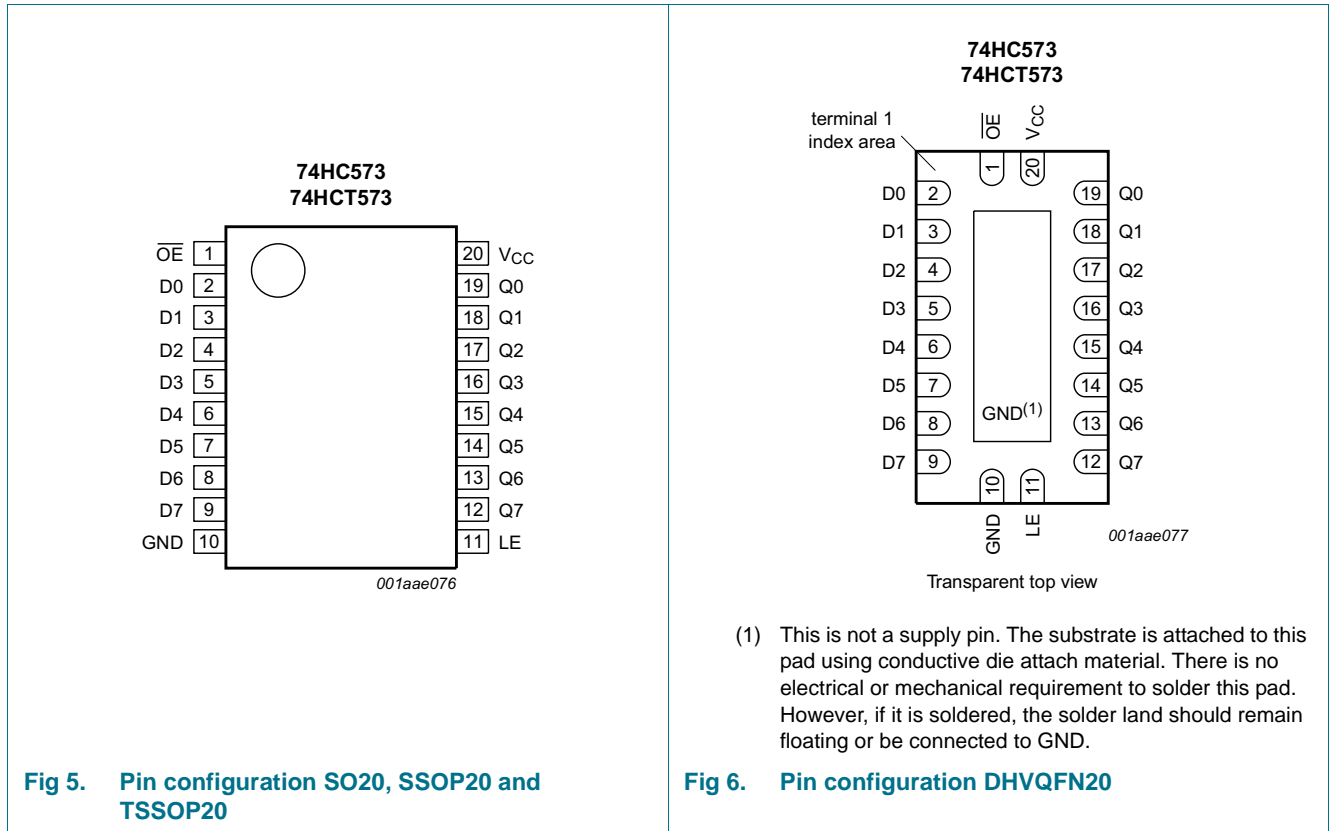


Fig 3. Logic symbol

Fig 4. IEC logic symbol

## 5. Pinning information

### 5.1 Pinning



### 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{OE}$	1	3-state output enable input (active LOW)
D[0:7]	2, 3, 4, 5, 6, 7, 8, 9	data input
GND	10	ground (0 V)
LE	11	latch enable input (active HIGH)
Q[0:7]	19, 18, 17, 16, 15, 14, 13, 12	3-state latch output
V <sub>CC</sub>	20	supply voltage

## 6. Functional description

Table 3. Function table<sup>[1]</sup>

Operating mode	Control		Input	Internal latches	Output
	$\overline{\text{OE}}$	LE	Dn		Qn
Enable and read register (transparent mode)	L	H	L	L	L
			H	H	H
Latch and read register	L	L	l	L	L
			h	H	H
Latch register and disable outputs	H	L	l	L	Z
			h	H	Z

- [1] H = HIGH voltage level;  
 h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition;  
 L = LOW voltage level;  
 l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition;  
 Z = high-impedance OFF-state.

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7	V
$I_{IK}$	input clamping current	$V_I < -0.5 \text{ V}$ or $V_I > V_{CC} + 0.5 \text{ V}$	-	$\pm 20$	mA
$I_{OK}$	output clamping current	$V_O < -0.5 \text{ V}$ or $V_O > V_{CC} + 0.5 \text{ V}$	-	$\pm 20$	mA
$I_O$	output current	$V_O = -0.5 \text{ V}$ to $(V_{CC} + 0.5 \text{ V})$	-	$\pm 35$	mA
$I_{CC}$	supply current		-	+70	mA
$I_{GND}$	ground current		-70	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	SO20, SSOP20, TSSOP20 and DHVQFN20 packages <sup>[1]</sup>	-	500	mW

- [1] For SO20:  $P_{tot}$  derates linearly with 8 mW/K above 70 °C.  
 For SSOP20 and TSSOP20 packages:  $P_{tot}$  derates linearly with 5.5 mW/K above 60 °C.  
 For DHVQFN20 package:  $P_{tot}$  derates linearly with 4.5 mW/K above 60 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC573			74HCT573			Unit
			Min	Typ	Max	Min	Typ	Max	
$V_{CC}$	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
$V_I$	input voltage		0	-	$V_{CC}$	0	-	$V_{CC}$	V
$V_O$	output voltage		0	-	$V_{CC}$	0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0\text{ V}$	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5\text{ V}$	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0\text{ V}$	-	-	83	-	-	-	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HC573</b>										
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 2.0\text{ V}$	1.5	1.2	-	1.5	-	1.5	-	V
		$V_{CC} = 4.5\text{ V}$	3.15	2.4	-	3.15	-	3.15	-	V
		$V_{CC} = 6.0\text{ V}$	4.2	3.2	-	4.2	-	4.2	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 2.0\text{ V}$	-	0.8	0.5	-	0.5	-	0.5	V
		$V_{CC} = 4.5\text{ V}$	-	2.1	1.35	-	1.35	-	1.35	V
		$V_{CC} = 6.0\text{ V}$	-	2.8	1.8	-	1.8	-	1.8	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$								
		$I_O = -20\text{ }\mu\text{A}$ ; $V_{CC} = 2.0\text{ V}$	1.9	2.0	-	1.9	-	1.9	-	V
		$I_O = -20\text{ }\mu\text{A}$ ; $V_{CC} = 4.5\text{ V}$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -20\text{ }\mu\text{A}$ ; $V_{CC} = 6.0\text{ V}$	5.9	6.0	-	5.9	-	5.9	-	V
		$I_O = -6.0\text{ mA}$ ; $V_{CC} = 4.5\text{ V}$	3.98	4.32	-	3.84	-	3.7	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$								
		$I_O = 20\text{ }\mu\text{A}$ ; $V_{CC} = 2.0\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20\text{ }\mu\text{A}$ ; $V_{CC} = 4.5\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20\text{ }\mu\text{A}$ ; $V_{CC} = 6.0\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 6.0\text{ mA}$ ; $V_{CC} = 4.5\text{ V}$	-	0.15	0.26	-	0.33	-	0.4	V
$I_{OZ}$	OFF-state output current	$I_O = 7.8\text{ mA}$ ; $V_{CC} = 6.0\text{ V}$	-	0.16	0.26	-	0.33	-	0.4	V
		$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 6.0\text{ V}$ ; $V_O = V_{CC}$ or GND	-	-	$\pm 0.5$	-	$\pm 5.0$	-	$\pm 10.0$	$\mu\text{A}$
$I_I$	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0\text{ V}$	-	-	$\pm 0.1$	-	$\pm 1.0$	-	$\pm 1.0$	$\mu\text{A}$

**Table 6. Static characteristics ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$I_{CC}$	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0$ V	-	-	8.0	-	80	-	160	$\mu$ A
$C_I$	input capacitance		-	3.5	-					pF
<b>74HCT573</b>										
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5$ V								
		$I_O = -20$ $\mu$ A	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -6$ mA	3.98	4.32	-	3.84	-	3.7	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5$ V								
		$I_O = 20$ $\mu$ A	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 6.0$ mA	-	0.16	0.26	-	0.33	-	0.4	V
$I_I$	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5$ V	-	-	$\pm 0.1$	-	$\pm 1.0$	-	$\pm 1.0$	$\mu$ A
$I_{OZ}$	OFF-state output current	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 5.5$ V; $V_O = V_{CC}$ or GND	-	-	$\pm 0.5$	-	$\pm 5.0$	-	$\pm 10$	$\mu$ A
$I_{CC}$	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	8.0	-	80	-	160	$\mu$ A
$\Delta I_{CC}$	additional supply current	$V_I = V_{CC} - 2.1$ V; other inputs at $V_{CC}$ or GND; $V_{CC} = 4.5$ V to 5.5 V; $I_O = 0$ A								
		per input pin; Dn inputs	-	35	126	-	158	-	172	$\mu$ A
		per input pin; LE input	-	65	234	-	293	-	319	$\mu$ A
		per input pin; $\overline{OE}$ input	-	125	450	-	563	-	613	$\mu$ A
$C_I$	input capacitance		-	3.5	-	-	-	-	-	pF

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V);  $C_L = 50$  pF unless otherwise specified; for test circuit see [Figure 11](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HC573</b>										
$t_{pd}$	propagation delay	Dn to Qn; see <a href="#">Figure 7</a> [1]								
		$V_{CC} = 2.0$ V	-	47	150	-	190	-	225	ns
		$V_{CC} = 4.5$ V	-	17	30	-	38	-	45	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	14	-	-	-	-	-	ns
		$V_{CC} = 6.0$ V	-	14	26	-	33	-	38	ns
$t_{pd}$	propagation delay	LE to Qn; see <a href="#">Figure 8</a> [1]								
		$V_{CC} = 2.0$ V	-	50	150	-	190	-	225	ns
		$V_{CC} = 4.5$ V	-	18	30	-	38	-	45	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	15	-	-	-	-	-	ns
		$V_{CC} = 6.0$ V	-	14	26	-	33	-	38	ns
$t_{en}$	enable time	OE to Qn; see <a href="#">Figure 9</a> [2]								
		$V_{CC} = 2.0$ V	-	44	140	-	175	-	210	ns
		$V_{CC} = 4.5$ V	-	16	28	-	35	-	42	ns
		$V_{CC} = 6.0$ V	-	13	24	-	30	-	36	ns
$t_{dis}$	disable time	OE to Qn; see <a href="#">Figure 9</a> [3]								
		$V_{CC} = 2.0$ V	-	55	150	-	190	-	225	ns
		$V_{CC} = 4.5$ V	-	20	30	-	38	-	45	ns
		$V_{CC} = 6.0$ V	-	16	26	-	33	-	38	ns
$t_t$	transition time	Qn; see <a href="#">Figure 7</a> [4]								
		$V_{CC} = 2.0$ V	-	14	60	-	75	-	90	ns
		$V_{CC} = 4.5$ V	-	5	12	-	15	-	18	ns
		$V_{CC} = 6.0$ V	-	4	10	-	13	-	15	ns
$t_w$	pulse width	LE HIGH; see <a href="#">Figure 8</a>								
		$V_{CC} = 2.0$ V	80	14	-	100	-	120	-	ns
		$V_{CC} = 4.5$ V	16	5	-	20	-	24	-	ns
		$V_{CC} = 6.0$ V	14	4	-	17	-	20	-	ns
$t_{su}$	set-up time	Dn to LE; see <a href="#">Figure 10</a>								
		$V_{CC} = 2.0$ V	50	11	-	65	-	75	-	ns
		$V_{CC} = 4.5$ V	10	4	-	13	-	15	-	ns
		$V_{CC} = 6.0$ V	9	3	-	11	-	13	-	ns
$t_h$	hold time	Dn to LE; see <a href="#">Figure 10</a>								
		$V_{CC} = 2.0$ V	5	3	-	5	-	5	-	ns
		$V_{CC} = 4.5$ V	5	1	-	5	-	5	-	ns
		$V_{CC} = 6.0$ V	5	1	-	5	-	5	-	ns
$C_{PD}$	power dissipation capacitance	$C_L = 50$ pF; $f = 1$ MHz; $V_1 = \text{GND to } V_{CC}$ [5]	-	26	-	-	-	-	-	pF



**Table 7. Dynamic characteristics ...continued**

Voltages are referenced to GND (ground = 0 V);  $C_L = 50$  pF unless otherwise specified; for test circuit see [Figure 11](#).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HCT573</b>										
$t_{pd}$	propagation delay	Dn to Qn; see <a href="#">Figure 7</a> [1]								
		$V_{CC} = 4.5$ V	-	20	35	-	44	-	53	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	17	-	-	-	-	-	ns
$t_{pd}$	propagation delay	LE to Qn; see <a href="#">Figure 8</a> [1]								
		$V_{CC} = 4.5$ V	-	18	35	-	44	-	53	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	15	-	-	-	-	-	ns
$t_{en}$	enable time	$\overline{OE}$ to Qn; see <a href="#">Figure 9</a> [2]								
		$V_{CC} = 4.5$ V	-	17	30	-	38	-	45	ns
$t_{dis}$	disable time	$\overline{OE}$ to Qn; see <a href="#">Figure 9</a> [3]								
		$V_{CC} = 4.5$ V	-	18	30	-	38	-	45	ns
$t_t$	transition time	Qn; see <a href="#">Figure 7</a> [4]								
		$V_{CC} = 4.5$ V	-	5	12	-	15	-	18	ns
$t_W$	pulse width	LE HIGH; see <a href="#">Figure 8</a>								
		$V_{CC} = 4.5$ V	16	5	-	20	-	24	-	ns
$t_{su}$	set-up time	Dn to LE; see <a href="#">Figure 10</a>								
		$V_{CC} = 4.5$ V	13	7	-	16	-	20	-	ns
$t_h$	hold time	Dn to LE; see <a href="#">Figure 10</a>								
		$V_{CC} = 4.5$ V	9	4	-	11	-	15	-	ns
$C_{PD}$	power dissipation capacitance	$C_L = 50$ pF; $f = 1$ MHz; $V_I = GND$ to $V_{CC} - 1.5$ V [5]	-	26	-	-	-	-	-	pF

[1]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .

[2]  $t_{en}$  is the same as  $t_{PZH}$  and  $t_{PZL}$ .

[3]  $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ .

[4]  $t_t$  is the same as  $t_{THL}$  and  $t_{TLH}$ .

[5]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu$ W).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

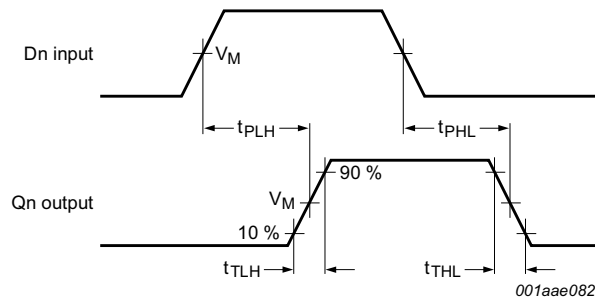
$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in V;

$N$  = number of inputs switching;

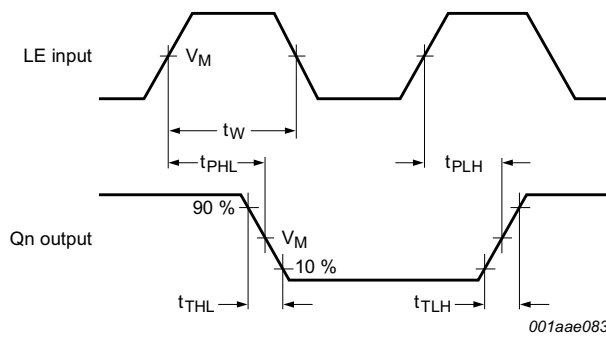
$\sum(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

11. Waveforms



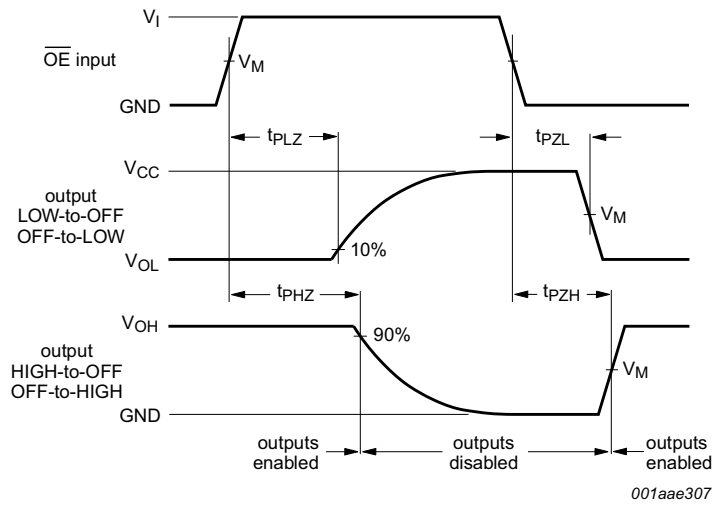
Measurement points are given in [Table 8](#).

Fig 7. Propagation delay data input (Dn) to output (Qn) and output transition time



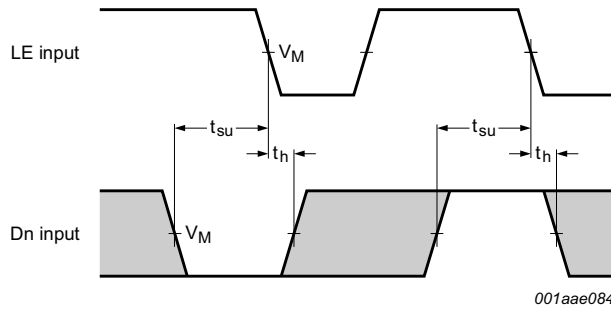
Measurement points are given in [Table 8](#).

Fig 8. Pulse width latch enable input (LE), propagation delay latch enable input (LE) to output (Qn) and output transition time



Measurement points are given in [Table 8](#).  
 $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 9. Enable and disable times**

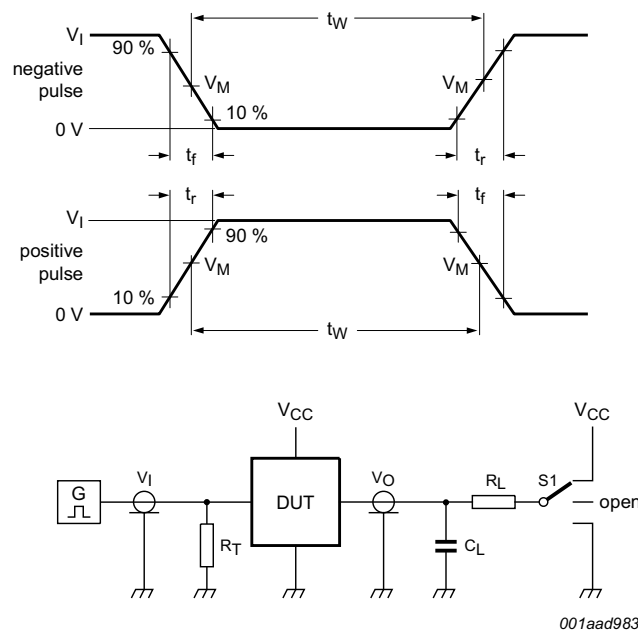


Measurement points are given in [Table 8](#).  
 The shaded areas indicate when the input is permitted to change for predictable output performance.

**Fig 10. Set-up and hold times for data input (Dn) to latch input (LE)**

**Table 8. Measurement points**

Type	Input	Output
	$V_M$	$V_M$
74HC573	$0.5V_{CC}$	$0.5V_{CC}$
74HCT573	1.3 V	1.3 V



Test data is given in [Table 9](#).

Definitions test circuit:

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_L$  = Load resistance.

S1 = Test selection switch.

**Fig 11. Test circuit for measuring switching times**

**Table 9. Test data**

Type	Input		Load		S1 position		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
74HC573	$V_{CC}$	6 ns	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$
74HCT573	3 V	6 ns	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$

## 12. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

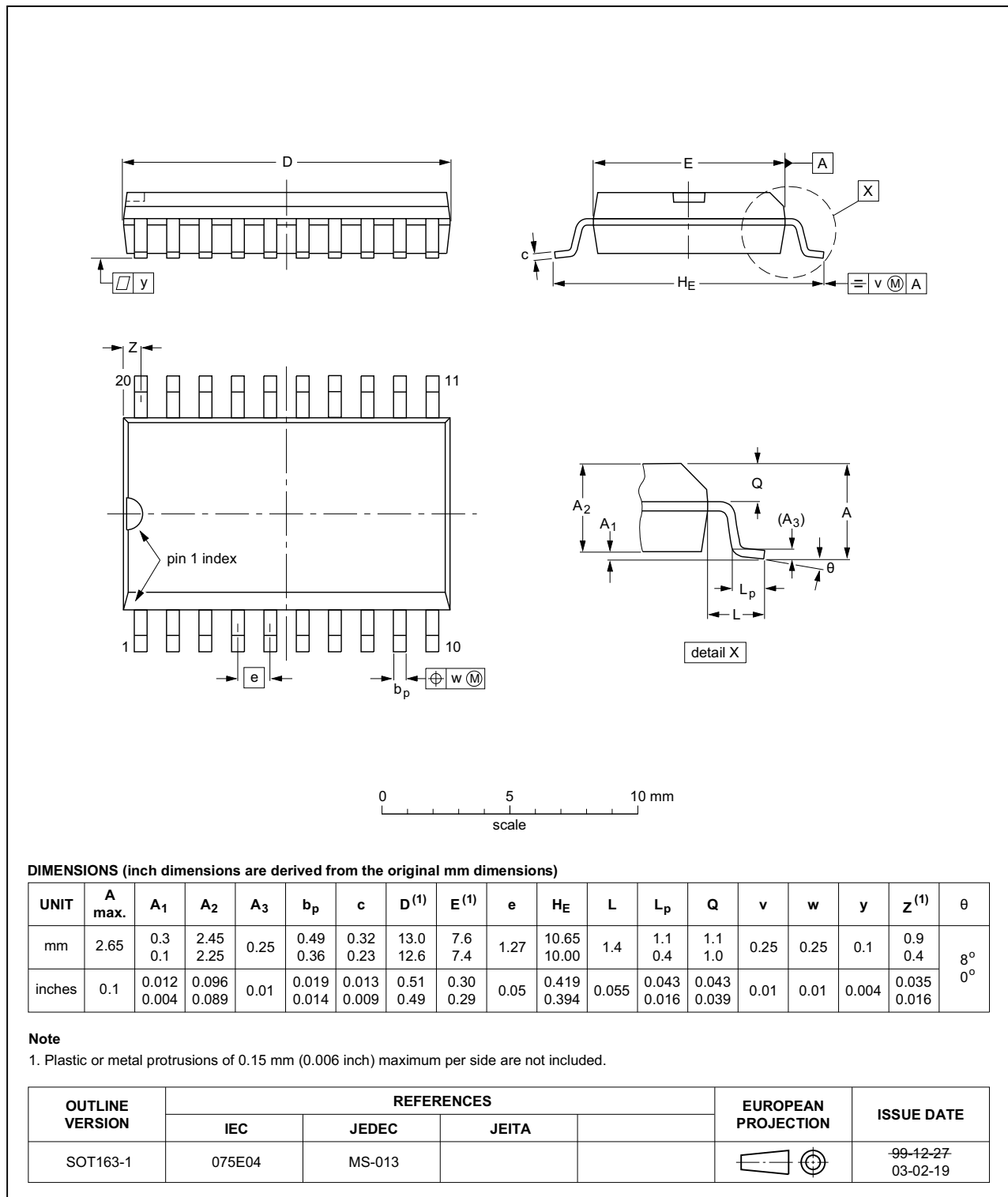


Fig 12. Package outline SOT163-1 (SO20)

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1

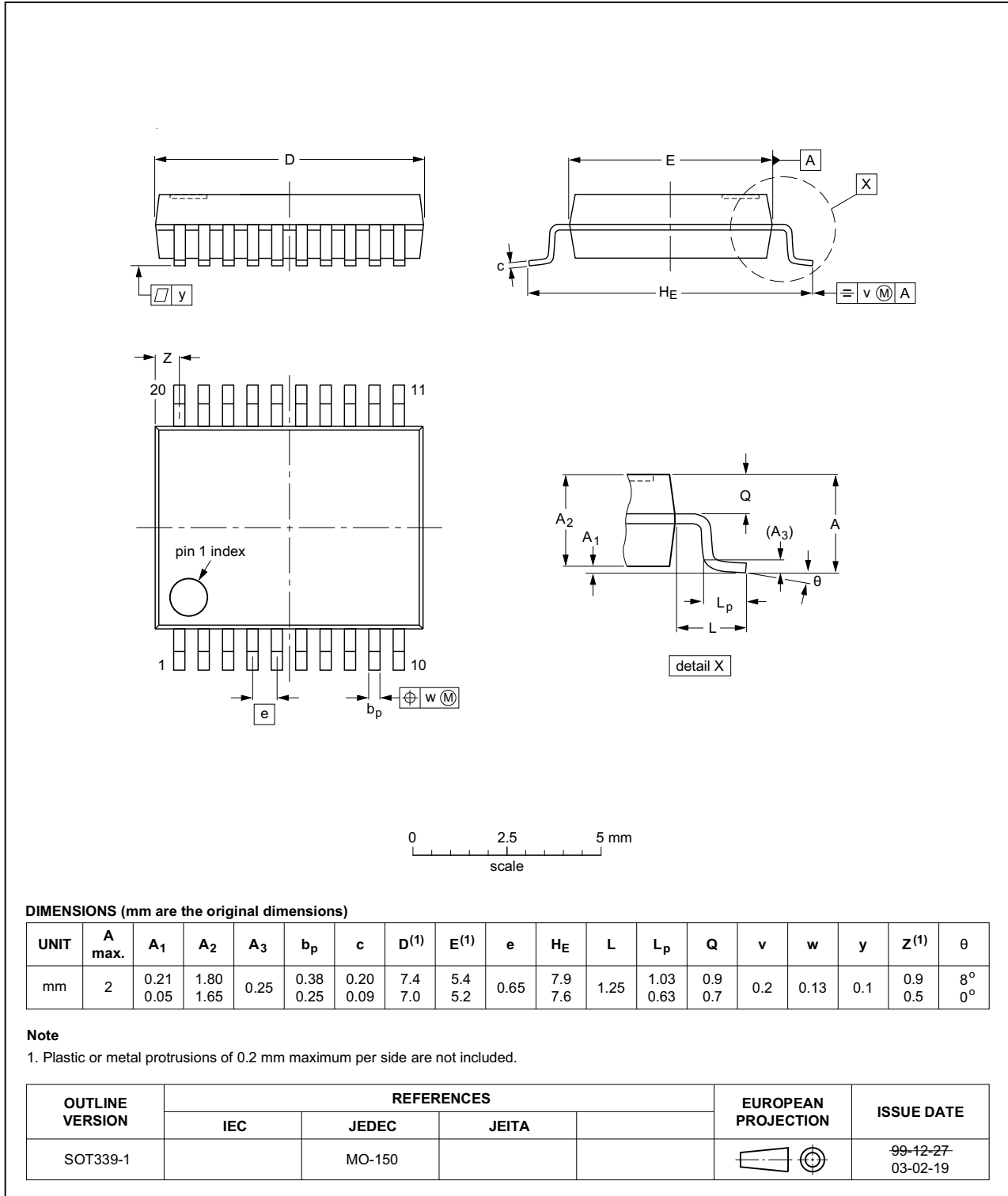


Fig 13. Package outline SOT339-1 (SSOP20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

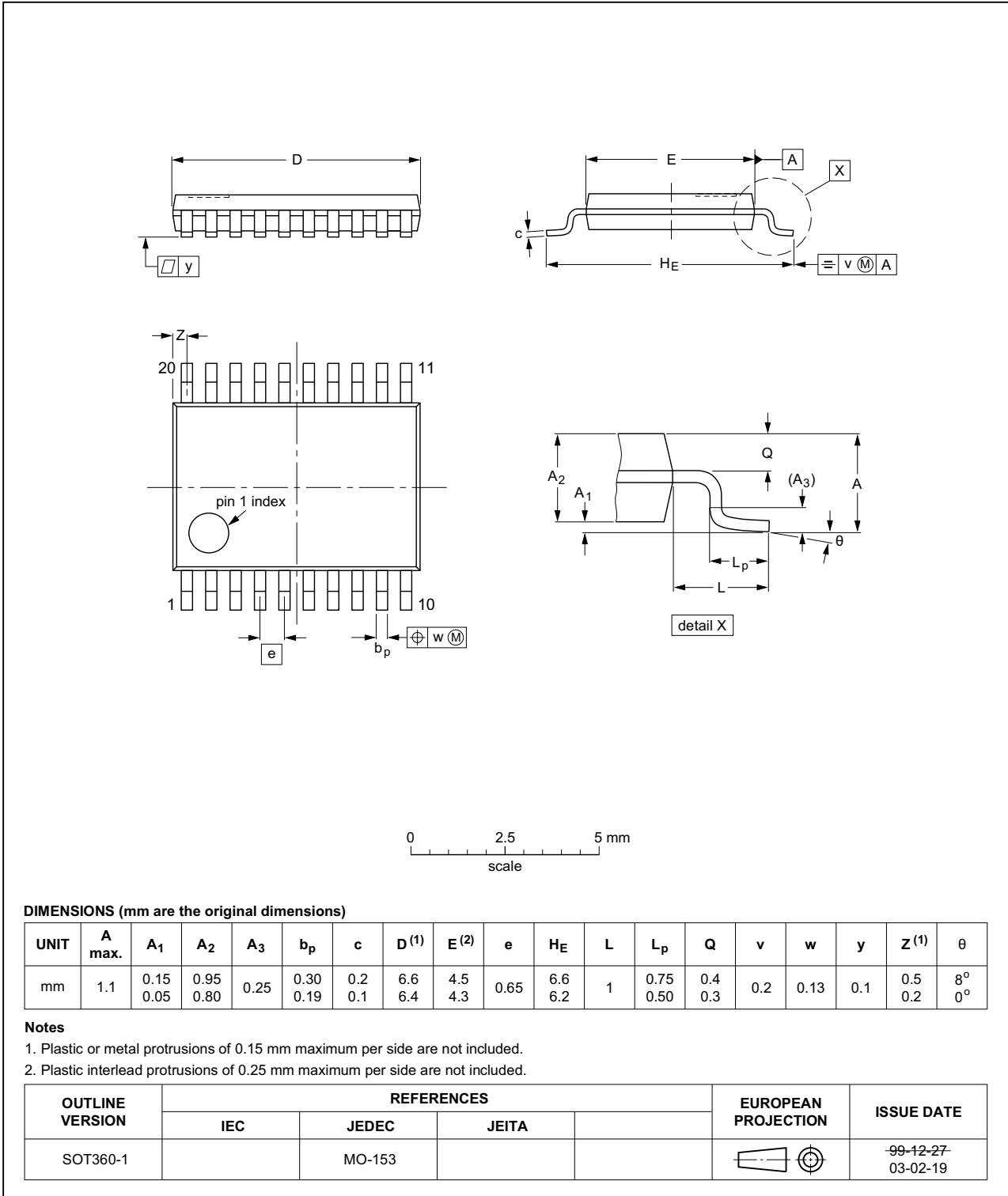


Fig 14. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;  
20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1



Fig 15. Package outline SOT764-1 (DHVQFN20)



## 13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT573 v.7	20160304	Product data sheet	-	74HC_HCT573 v.6
Modifications:	<ul style="list-style-type: none"> <li>Type numbers 74HC573N and 74HCT573N (SOT146-1) removed.</li> </ul>			
74HC_HCT573 v.6	20150126	Product data sheet	-	74HC_HCT573 v.5
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Table 7</a>: Power dissipation capacitance condition for 74HCT573 is corrected.</li> </ul>			
74HC_HCT573 v.5	20120815	Product data sheet	-	74HC_HCT573 v.4
Modifications:	<ul style="list-style-type: none"> <li>Alternative descriptive title corrected (errata).</li> </ul>			
74HC_HCT573 v.4	20120806	Product data sheet	-	74HC_HCT573 v.3
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>			
74HC_HCT573 v.3	20060117	Product data sheet	-	74HC_HCT573_CNV v.2
74HC_HCT573_CNV v.2	19901201	Product specification	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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