Atmel SAM D20J / SAM D20G / SAM D20E

ARM-Based Microcontroller

DATASHEET SUMMARY

Description

The Atmel® SAM D20 is a series of low-power microcontrollers using the 32-bit ARM® Cortex®-M0+ processor, and ranging from 32- to 64-pins with up to 256KB Flash and 32KB of SRAM. The SAM D20 devices operate at a maximum frequency of 48MHz and reach 2.14 Coremark/MHz. They are designed for simple and intuitive migration with identical peripheral modules, hex compatible code, identical linear address map and pin compatible migration paths between all devices in the product series. All devices include intelligent and flexible peripherals, Atmel Event System for inter-peripheral signaling, and support for capacitive touch button, slider and wheel user interfaces.

The Atmel SAM D20 devices provide the following features: In-system programmable Flash, eight-channel Event System, programmable interrupt controller, up to 52 programmable I/O pins, 32-bit real-time clock and calendar, up to eight 16-bit Timer/Counters (TC). The timer/counters can be configured to perform frequency and waveform generation, program execution timing or input capture with time and frequency measurement of digital signals. The TCs can operate in 8- or 16-bit mode, or be cascaded to form a 32-bit TC. The series provide up to six Serial Communication Modules (SERCOM) that each can be configured to act as an USART, UART, SPI and I^2C up to 400kHz; up to twenty-channel 350ksps 12-bit ADC with programmable gain and optional oversampling and decimation supporting up to 16-bit resolution, one 10-bit 350ksps DAC, two analog comparators with window mode, Peripheral Touch Controller supporting up to 256 buttons, sliders, wheels, and proximity sensing; programmable Watchdog Timer, brown-out detector and power-on reset, and two-pin Serial Wire Debug (SWD) program and debug interface.

All devices have accurate and low-power external and internal oscillators. All oscillators can be used as a source for the system clock. Different clock domains can be independently configured to run at different frequencies while enabling power saving by running each peripheral at its optimal clock frequency.

The SAM D20 devices have two software-selectable sleep modes, idle and standby. In idle mode the CPU is stopped while all other functions can be kept running. In standby all clocks and functions are stopped expect those selected to continue running. The device supports SleepWalking, which is the module's ability to wake itself up and wake up its own clock, and hence perform predefined tasks without waking up the CPU. The CPU can then be only woken on a need basis, e.g. a threshold is crossed or a result is ready. The Event System supports synchronous and asynchronous events, allowing peripherals to receive, react to and send events even in standby mode.

The Flash program memory can be reprogrammed in-system through the SWD interface. The same interface can be used for non-intrusive on-chip debug of application code. A boot loader running in the device can use any communication interface to download and upgrade the application program in the Flash memory.

The Atmel SAM D20 devices are supported with a full suite of program and system development tools, including C compilers, macro assemblers, program debugger/simulators, programmers and evaluation kits.

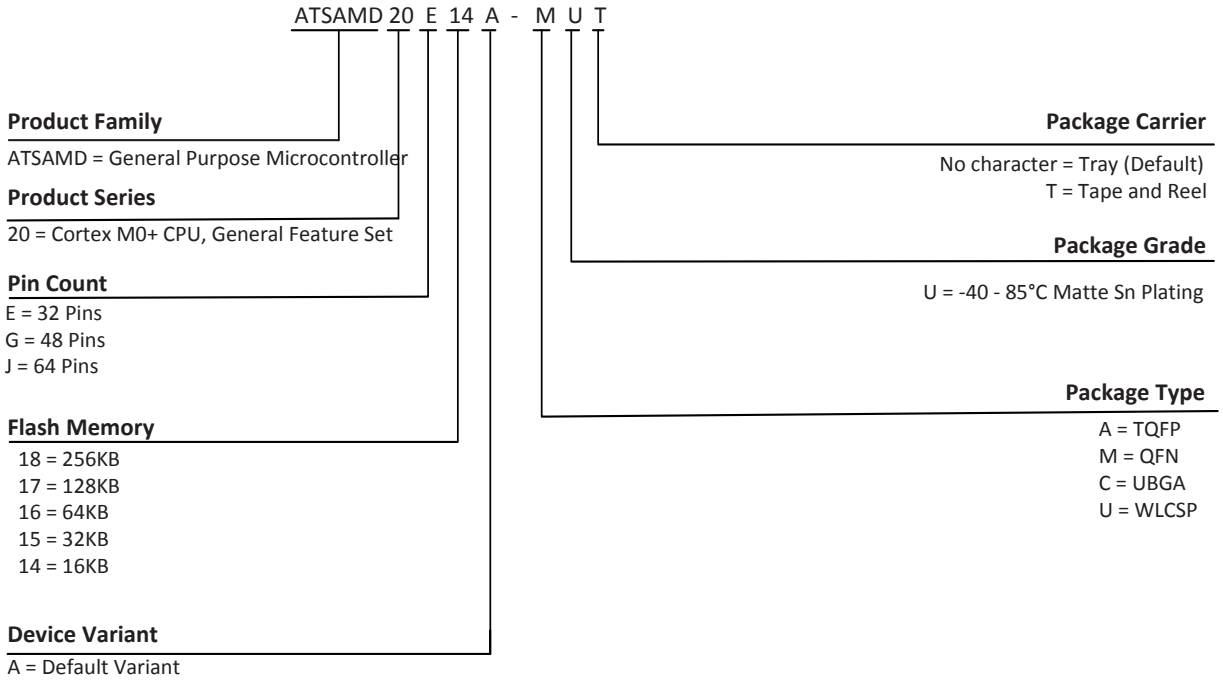
Features

- Processor
  - ARM Cortex-M0+ CPU running at up to 48MHz
    - Single-cycle hardware multiplier
- Memories
  - 16/32/64/128/256KB in-system self-programmable flash
  - 2/4/8/16/32KB SRAM
- System
  - Power-on reset (POR) and brown-out detection (BOD)
  - Internal and external clock options with 48MHz Digital Frequency Locked Loop (DFLL48M)
  - External Interrupt Controller (EIC)
  - 16 external interrupts
  - One non-maskable interrupt
  - Two-pin Serial Wire Debug (SWD) programming, test and debugging interface
- Low Power
  - Idle and standby sleep modes
  - SleepWalking peripherals
- Peripherals
  - 8-channel Event System
  - Up to eight 16-bit Timer/Counters (TC), configurable as either:
    - One 16-bit TC with compare/capture channels
    - One 8-bit TC with compare/capture channels
    - One 32-bit TC with compare/capture channels, by using two TCs
  - 32-bit Real Time Counter (RTC) with clock/calendar function
  - Watchdog Timer (WDT)
  - CRC-32 generator
  - Up to six Serial Communication Interfaces (SERCOM), each configurable to operate as either:
    - USART with full-duplex and single-wire half-duplex configuration
    - I^2C up to 400kHz
    - SPI
  - One 12-bit, 350ksps Analog-to-Digital Converter (ADC) with up to 20 channels
    - Differential and single-ended channels
    - 1/2x to 16x gain stage
    - Automatic offset and gain error compensation
    - Oversampling and decimation in hardware to support 13-, 14-, 15- or 16-bit resolution
  - 10-bit, 350ksps Digital-to-Analog Converter (DAC)
  - Two Analog Comparators with window compare function
  - Peripheral Touch Controller (PTC)
    - 256-Channel capacitive touch and proximity sensing
- I/O
  - Up to 52 programmable I/O pins
- Packages
  - 64-pin TQFP, QFN
  - 48-pin TQFP, QFN
  - 32-pin TQFP, QFN
- Operating Voltage
  - 1.62V – 3.63V
- Power Consumption
  - Down to 70µA/MHz in active mode
  - Down to 8µA running the Peripheral Touch Controller

1. Configuration Summary

	SAM D20J	SAM D20G	SAM D20E
Number of pins	64	48	32
General Purpose I/O-pins (GPIOs)	52	38	26
Flash	256/128/64/32/16KB	256/128/64/32/16KB	256/128/64/32/16KB
SRAM	32/16/8/4/2KB	32/16/8/4/2KB	32/16/8/4/2KB
Maximum CPU frequency	48MHz		
Event System channels	8	8	8
Timer Counter (TC)	8	6	6
Waveform output channels for TC	2	2	2
Serial Communication Interface (SERCOM)	6	6	4
Analog-to-Digital Converter (ADC) channels	20	14	10
Analog comparators	2	2	2
Digital-to-Analog Converter (DAC) channels	1	1	1
Real-Time Counter (RTC)	Yes	Yes	Yes
RTC alarms	1	1	1
RTC compare values	1 32-bit value or 2 16-bit values	1 32-bit value or 2 16-bit values	1 32-bit value or 2 16-bit values
External Interrupt lines	16	16	16
Peripheral Touch Controller (PTC) X and Y lines	16x16	12x10	10x6
Packages	QFN TQFP	QFN TQFP	QFN TQFP
Oscillators	32.768kHz crystal oscillator (XOSC32K) 0.4-32MHz crystal oscillator (XOSC) 32.768kHzinternal oscillator (OSC32K) 32kHz ultra-low-power internal oscillator (OSCULP32K) 8MHz high-accuracy internal oscillator (OSC8M) 48MHz Digital Frequency Locked Loop (DFLL48M)		
SW Debug Interface	Yes	Yes	Yes
Watchdog Timer (WDT)	Yes	Yes	Yes

2. Ordering Information



2.1 SAM D20E

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMD20E14A-AU	16K	2K	TQFP32	Tray
ATSAMD20E14A-AUT				Tape & Reel
ATSAMD20E14A-MU			QFN32	Tray
ATSAMD20E14A-MUT				Tape & Reel
ATSAMD20E15A-AU	32K	4K	TQFP32	Tray
ATSAMD20E15A-AUT				Tape & Reel
ATSAMD20E15A-MU			QFN32	Tray
ATSAMD20E15A-MUT				Tape & Reel
ATSAMD20E16A-AU	64K	8K	TQFP32	Tray
ATSAMD20E16A-AUT				Tape & Reel
ATSAMD20E16A-MU			QFN32	Tray
ATSAMD20E16A-MUT				Tape & Reel
ATSAMD20E17A-AU	128K	16K	TQFP32	Tray
ATSAMD20E17A-AUT				Tape & Reel
ATSAMD20E17A-MU			QFN32	Tray
ATSAMD20E17A-MUT				Tape & Reel

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMD20E18A-AU	256K	32K	TQFP32	Tray
ATSAMD20E18A-AUT				Tape & Reel
ATSAMD20E18A-MU			QFN32	Tray
ATSAMD20E18A-MUT				Tape & Reel

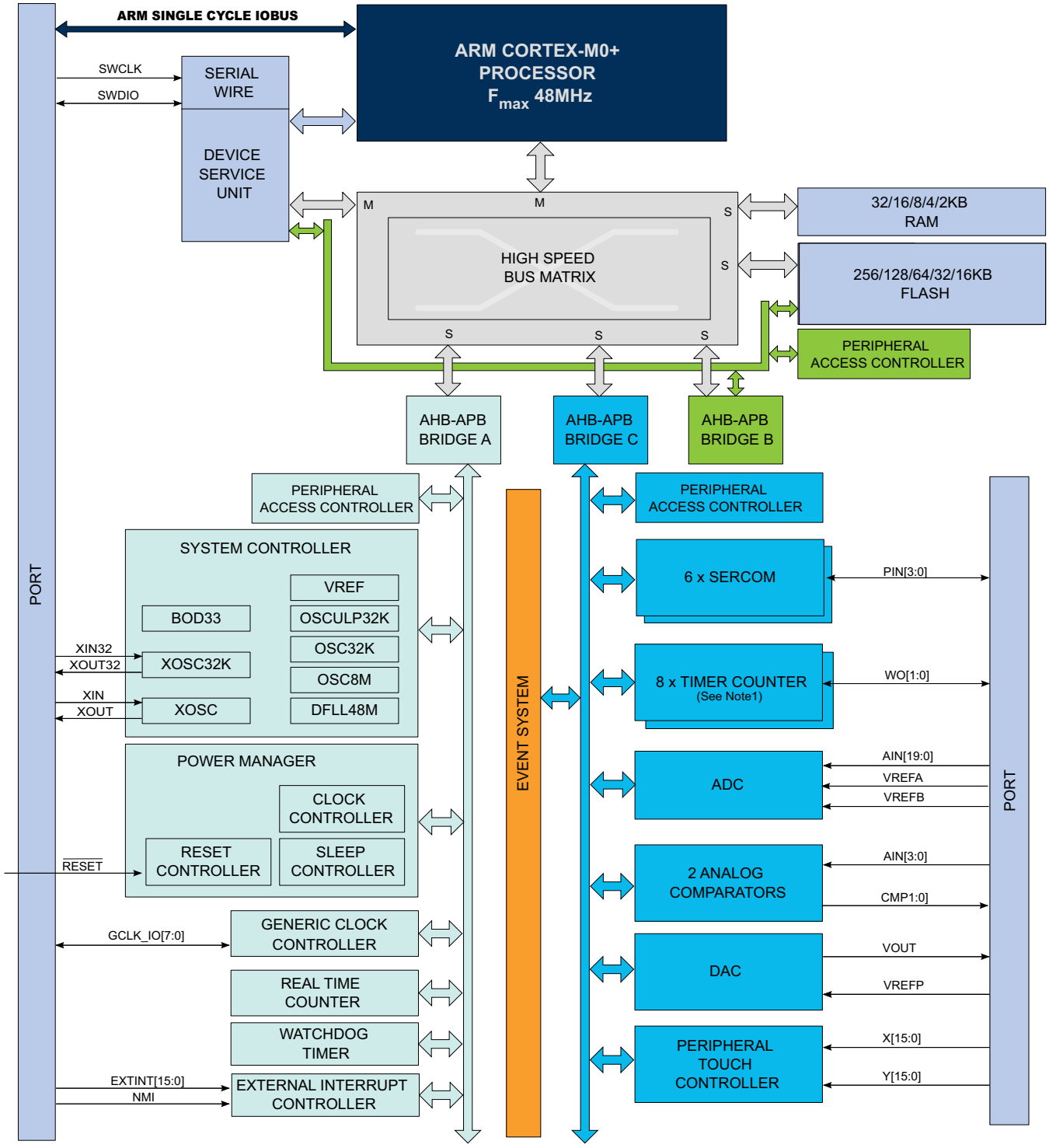
2.2 SAM D20G

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMD20G14A-AU	16K	2K	TQFP48	Tray
ATSAMD20G14A-AUT				Tape & Reel
ATSAMD20G14A-MU			QFN48	Tray
ATSAMD20G14A-MUT				Tape & Reel
ATSAMD20G15A-AU	32K	4K	TQFP48	Tray
ATSAMD20G15A-AUT				Tape & Reel
ATSAMD20G15A-MU			QFN48	Tray
ATSAMD20G15A-MUT				Tape & Reel
ATSAMD20G16A-AU	64K	8K	TQFP48	Tray
ATSAMD20G16A-AUT				Tape & Reel
ATSAMD20G16A-MU			QFN48	Tray
ATSAMD20G16A-MUT				Tape & Reel
ATSAMD20G17A-AU	128K	16K	TQFP48	Tray
ATSAMD20G17A-AUT				Tape & Reel
ATSAMD20G17A-MU			QFN48	Tray
ATSAMD20G17A-MUT				Tape & Reel
ATSAMD20G18A-AU	256K	32K	TQFP48	Tray
ATSAMD20G18A-AUT				Tape & Reel
ATSAMD20G18A-MU			QFN48	Tray
ATSAMD20G18A-MUT				Tape & Reel

2.3 SAM D20J

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMD20J14A-AU	16K	2K	TQFP64	Tray
ATSAMD20J14A-AUT				Tape & Reel
ATSAMD20J14A-MU			QFN64	Tray
ATSAMD20J14A-MUT				Tape & Reel
ATSAMD20J15A-AU	32K	4K	TQFP64	Tray
ATSAMD20J15A-AUT				Tape & Reel
ATSAMD20J15A-MU			QFN64	Tray
ATSAMD20J15A-MUT				Tape & Reel
ATSAMD20J16A-AU	64K	8K	TQFP64	Tray
ATSAMD20J16A-AUT				Tape & Reel
ATSAMD20J16A-MU			QFN64	Tray
ATSAMD20J16A-MUT				Tape & Reel
ATSAMD20J17A-AU	128K	16K	TQFP64	Tray
ATSAMD20J17A-AUT				Tape & Reel
ATSAMD20J17A-MU			QFN64	Tray
ATSAMD20J17A-MUT				Tape & Reel
ATSAMD20J18A-AU	256K	32K	TQFP64	Tray
ATSAMD20J18A-AUT				Tape & Reel
ATSAMD20J18A-MU			QFN64	Tray
ATSAMD20J18A-MUT				Tape & Reel

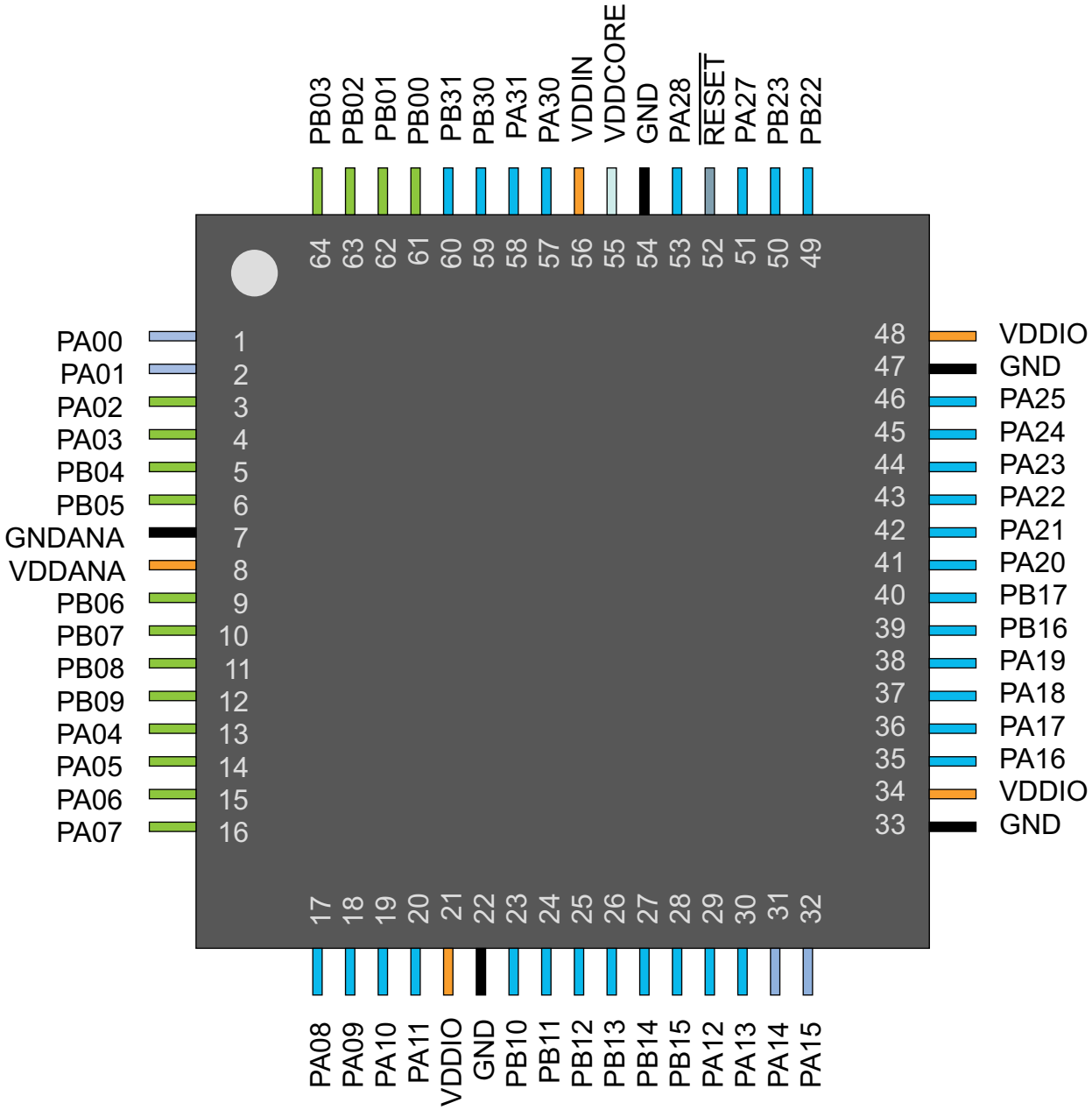
3. Block Diagram



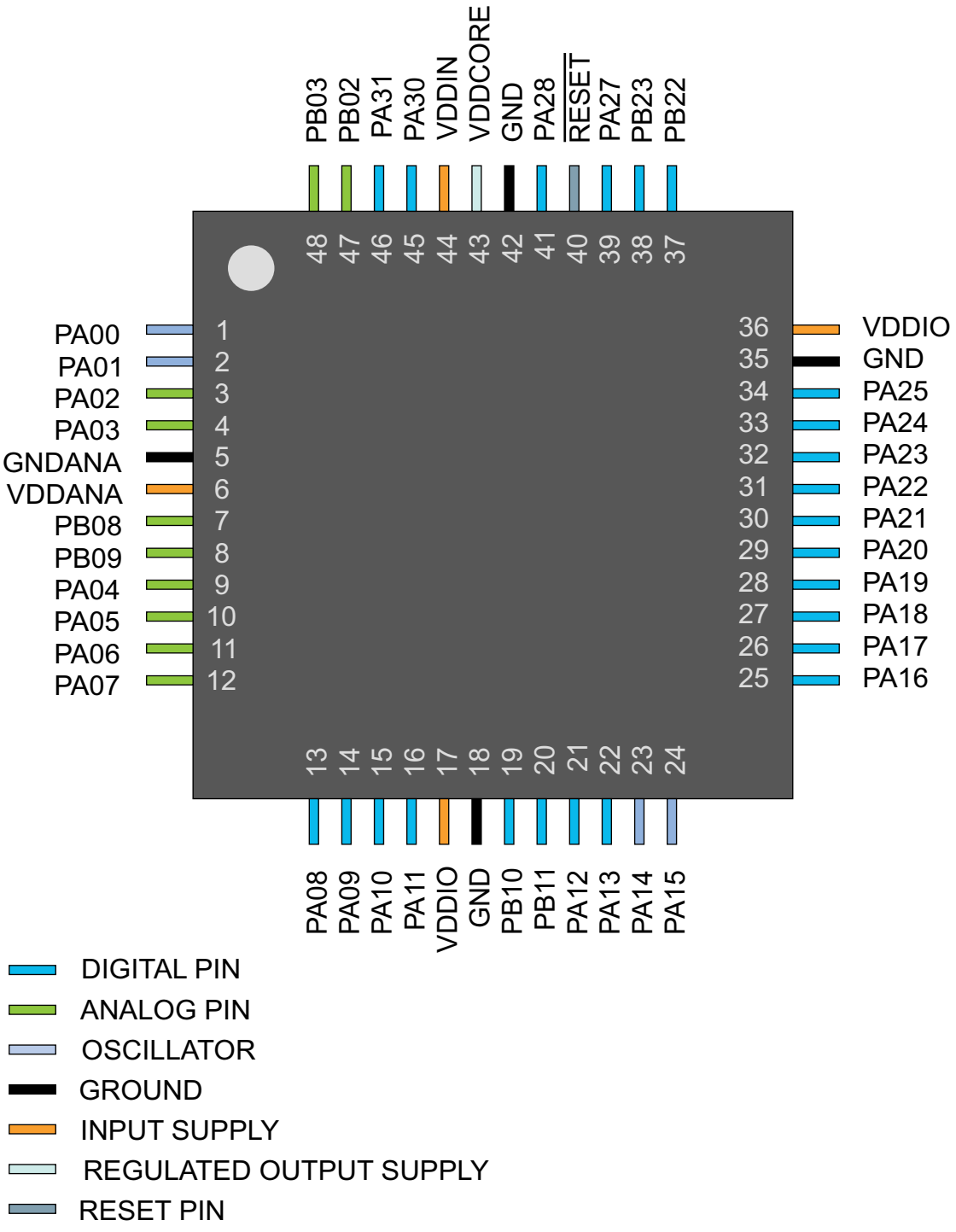
Notes: 1. Some products have different number of SERCOM instances, Timer/Counter instances, PTC signals and ADC signals. Refer to "Configuration Summary" on page 3 for details.

4. Pinout

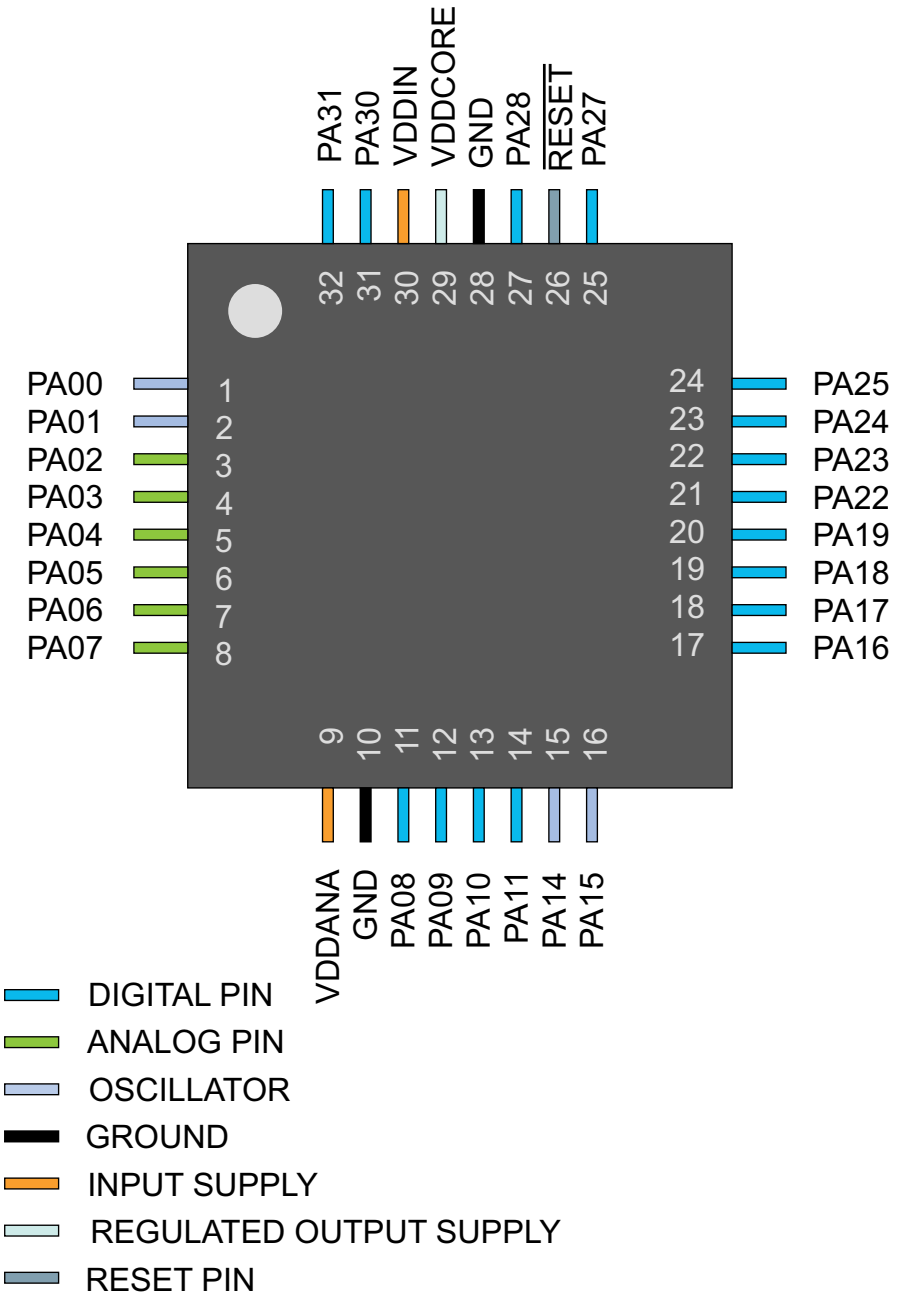
4.1 SAM D20J



4.2 SAM D20G


PB03
PB02
PA31
PA30
VDDIN
VDDCORE
GND
PA28
RESET
PA27
PB23
PB22
48
47
46
45
44
43
42
41
40
39
38
37
PA00
PA01
PA02
PA03
GNDANA
VDDANA
PB08
PB09
PA04
PA05
PA06
PA07
1
2
3
4
5
6
7
8
9
10
11
12
36
35
34
33
32
31
30
29
28
27
26
25
VDDIO
GND
PA25
PA24
PA23
PA22
PA21
PA20
PA19
PA18
PA17
PA16
13
14
15
16
17
18
19
20
21
22
23
24
PA08
PA09
PA10
PA11
VDDIO
GND
PB10
PB11
PA12
PA13
PA14
PA15
DIGITAL PIN
ANALOG PIN
OSCILLATOR
GROUND
INPUT SUPPLY
REGULATED OUTPUT SUPPLY
RESET PIN

4.3 SAM D20E


PA31
PA30
VDDIN
VDDCORE
GND
PA28
RESET
PA27
32
31
30
29
28
27
26
25
PA00
PA01
PA02
PA03
PA04
PA05
PA06
PA07
1
2
3
4
5
6
7
8
24
23
22
21
20
19
18
17
PA25
PA24
PA23
PA22
PA19
PA18
PA17
PA16
9
10
11
12
13
14
15
16
VDDANA
GND
PA08
PA09
PA10
PA11
PA14
PA15
DIGITAL PIN
ANALOG PIN
OSCILLATOR
GROUND
INPUT SUPPLY
REGULATED OUTPUT SUPPLY
RESET PIN

5. I/O Multiplexing and Considerations

5.1 Multiplexed Signals

Each pin is by default controlled by the PORT as a general purpose I/O and alternatively it can be assigned to one of the peripheral functions A, B, C, D, E, F, G or H. To enable a peripheral function on a pin, the Peripheral Multiplexer Enable bit in the Pin Configuration register corresponding to that pin (PINCFGn.PMUXEN, n = 0-31) in the PORT must be written to one. The selection of peripheral function A to H is done by writing to the Peripheral Multiplexing Odd and Even bits in the Peripheral Multiplexing register (PMUXn.PMUXE/O) in the PORT. Refer to !!!CRs_PORT_Top!!! for details on how to configure the I/O multiplexing.

Table 5-1 describes the peripheral signals multiplexed to the PORT I/O pins.

Table 5-1. PORT Function Multiplexing

Pin			I/O Pin	Supply	Pin Type	A	B[1]					C	D	E	F	G	H
SAM D20E	SAM D20G	SAM D20J				EIC	REF	ADC	AC	PTC	DAC	SERCOM[2]		TC[3]			AC/GCLK
1	1	1	PA00	VDDANA		EXTINT[0]							SERCOM1/ PAD[0]		TC2/ WO[0]		
2	2	2	PA01	VDDANA		EXTINT[1]							SERCOM1/ PAD[1]		TC2/ WO[1]		
3	3	3	PA02	VDDANA		EXTINT[2]		AIN[0]		Y[0]	VOUT						
4	4	4	PA03	VDDANA		EXTINT[3]	ADC/VREFA DAC/VREFA	AIN[1]		Y[1]							
		5	PB04	VDDANA		EXTINT[4]		AIN[12]		Y[10]							
		6	PB05	VDDANA		EXTINT[5]		AIN[13]		Y[11]							
		9	PB06	VDDANA		EXTINT[6]		AIN[14]		Y[12]							
		10	PB07	VDDANA		EXTINT[7]		AIN[15]		Y[13]							
	7	11	PB08	VDDANA		EXTINT[8]		AIN[2]		Y[14]			SERCOM4/ PAD[0]		TC4/ WO[0]		
	8	12	PB09	VDDANA		EXTINT[9]		AIN[3]		Y[15]			SERCOM4/ PAD[1]		TC4/ WO[1]		
5	9	13	PA04	VDDANA		EXTINT[4]	ADC/ VREFB	AIN[4]	AIN[0]	Y[2]			SERCOM0/ PAD[0]		TC0/ WO[0]		
6	10	14	PA05	VDDANA		EXTINT[5]		AIN[5]	AIN[1]	Y[3]			SERCOM0/ PAD[1]		TC0/ WO[1]		
7	11	15	PA06	VDDANA		EXTINT[6]		AIN[6]	AIN[2]	Y[4]			SERCOM0/ PAD[2]		TC1/ WO[0]		
8	12	16	PA07	VDDANA		EXTINT[7]		AIN[7]	AIN[3]	Y[5]			SERCOM0/ PAD[3]		TC1/ WO[1]		
11	13	17	PA08	VDDIO	I^2C	NMI		AIN[16]		X[0]		SERCOM0/ PAD[0]	SERCOM2/ PAD[0]	TC0/ WO[0]			
12	14	18	PA09	VDDIO	I^2C	EXTINT[9]		AIN[17]		X[1]		SERCOM0/ PAD[1]	SERCOM2/ PAD[1]	TC0/ WO[1]			
13	15	19	PA10	VDDIO		EXTINT[10]		AIN[18]		X[2]		SERCOM0/ PAD[2]	SERCOM2/ PAD[2]	TC1/ WO[0]			GCLK_O[4]
14	16	20	PA11	VDDIO		EXTINT[11]		AIN[19]		X[3]		SERCOM0/ PAD[3]	SERCOM2/ PAD[3]	TC1/ WO[1]			GCLK_IO[5]
	19	23	PB10	VDDIO		EXTINT[10]							SERCOM4/ PAD[2]		TC5/ WO[0]		GCLK_IO[4]
	20	24	PB11	VDDIO		EXTINT[11]							SERCOM4/ PAD[3]		TC5/ WO[1]		GCLK_IO[5]
		25	PB12	VDDIO	I^2C	EXTINT[12]				X[12]		SERCOM4/ PAD[0]		TC4/ WO[0]			GCLK_IO[6]
		26	PB13	VDDIO	I^2C	EXTINT[13]				X[13]		SERCOM4/ PAD[1]		TC4/ WO[1]			GCLK_IO[7]
		27	PB14	VDDIO		EXTINT[14]				X[14]		SERCOM4/ PAD[2]		TC5/ WO[0]			GCLK_IO[0]

Table 5-1. PORT Function Multiplexing (Continued)

Pin			I/O Pin	Supply	Pin Type	A	B[1]					C	D	E	F	G	H
SAM D20E	SAM D20G	SAM D20J				EIC	REF	ADC	AC	PTC	DAC	SERCOM[2]		TC[3]			AC/GCLK
		28	PB15	VDDIO		EXTINT[15]				X[15]		SERCOM4/ PAD[3]		TC5/ WO[1]			GCLK_IO[1]
	21	29	PA12	VDDIO	I^2C	EXTINT[12]						SERCOM2/ PAD[0]	SERCOM4/ PAD[0]	TC2/ WO[0]			AC/CMP[0]
	22	30	PA13	VDDIO	I^2C	EXTINT[13]						SERCOM2/ PAD[1]	SERCOM4/ PAD[1]	TC2/ WO[1]			AC/CMP[1]
15	23	31	PA14	VDDIO		EXTINT[14]						SERCOM2/ PAD[2]	SERCOM4/ PAD[2]	TC3/ WO[0]			GCLK_IO[0]
16	24	32	PA15	VDDIO		EXTINT[15]						SERCOM2/ PAD[3]	SERCOM4/ PAD[3]	TC3/ WO[1]			GCLK_IO[1]
17	25	35	PA16	VDDIO	I^2C	EXTINT[0]				X[4]		SERCOM1/ PAD[0]	SERCOM3/ PAD[0]		TC2/ WO[0]		GCLK_IO[2]
18	26	36	PA17	VDDIO	I^2C	EXTINT[1]				X[5]		SERCOM1/ PAD[1]	SERCOM3/ PAD[1]		TC2/ WO[1]		GCLK_IO[3]
19	27	37	PA18	VDDIO		EXTINT[2]				X[6]		SERCOM1/ PAD[2]	SERCOM3/ PAD[2]		TC3/ WO[0]		AC/CMP[0]
20	28	38	PA19	VDDIO		EXTINT[3]				X[7]		SERCOM1/ PAD[3]	SERCOM3/ PAD[3]		TC3/ WO[1]		AC/CMP[1]
		39	PB16	VDDIO	I^2C	EXTINT[0]						SERCOM5/ PAD[0]		TC6/ WO[0]			GCLK_IO[2]
		40	PB17	VDDIO	I^2C	EXTINT[1]						SERCOM5/ PAD[1]		TC6/ WO[1]			GCLK_IO[3]
	29	41	PA20	VDDIO		EXTINT[4]				X[8]		SERCOM5/ PAD[2]	SERCOM3/ PAD[2]	TC7/ WO[0]			GCLK_IO[4]
	30	42	PA21	VDDIO		EXTINT[5]				X[9]		SERCOM5/ PAD[3]	SERCOM3/ PAD[3]	TC7/ WO[1]			GCLK_IO[5]
21	31	43	PA22	VDDIO	I^2C	EXTINT[6]				X[10]		SERCOM3/ PAD[0]	SERCOM5/ PAD[0]		TC4/ WO[0]		GCLK_IO[6]
22	32	44	PA23	VDDIO	I^2C	EXTINT[7]				X[11]		SERCOM3/ PAD[1]	SERCOM5/ PAD[1]		TC4/ WO[1]		GCLK_IO[7]
23	33	45	PA24	VDDIO		EXTINT[12]						SERCOM3/ PAD[2]	SERCOM5/ PAD[2]		TC5/ WO[0]		
24	34	46	PA25	VDDIO		EXTINT[13]						SERCOM3/ PAD[3]	SERCOM5/ PAD[3]		TC5/ WO[1]		
	37	49	PB22	VDDIO		EXTINT[6]							SERCOM5/ PAD[2]		TC7/ WO[0]		GCLK_IO[0]
	38	50	PB23	VDDIO		EXTINT[7]							SERCOM5/ PAD[3]		TC7/ WO[1]		GCLK_IO[1]
25	39	51	PA27	VDDIO		EXTINT[15]											GCLK_IO[0]
27	41	53	PA28	VDDIO		EXTINT[8]											GCLK_IO[0]
31	45	57	PA30	VDDIO		EXTINT[10]							SERCOM1/ PAD[2]		TC1/ WO[0]	SWCLK	GCLK_IO[0]
32	46	58	PA31	VDDIO		EXTINT[11]							SERCOM1/ PAD[3]		TC1/ WO[1]	SWDIO[4]	
		59	PB30	VDDIO	I^2C	EXTINT[14]							SERCOM5/ PAD[0]		TC0/ WO[0]		
		60	PB31	VDDIO	I^2C	EXTINT[15]							SERCOM5/ PAD[1]		TC0/ WO[1]		
		61	PB00	VDDANA		EXTINT[0]		AIN[8]		Y[6]			SERCOM5/ PAD[2]		TC7/ WO[0]		
		62	PB01	VDDANA		EXTINT[1]		AIN[9]		Y[7]			SERCOM5/ PAD[3]		TC7/ WO[1]		
	47	63	PB02	VDDANA		EXTINT[2]		AIN[10]		Y[8]			SERCOM5/ PAD[0]		TC6/ WO[0]		
	48	64	PB03	VDDANA		EXTINT[3]		AIN[11]		Y[9]			SERCOM5/ PAD[1]		TC6/ WO[1]		

Note: 1. All analog pin functions are on peripheral function B. Peripheral function B must be selected to disable the digital control of the pin.

2. Only some pins can be used in SERCOM I^2C mode. See the Type column for using a SERCOM pin in I^2C mode. Refer to the !!!CRs_ElChar_I2C_Pins!!! for details on the I^2C pin characteristics
3. Note that TC6 and TC7 are not supported on the SAM D20G. Refer to "Configuration Summary" on page 3 for details.
4. This function is only activated in the presence of a debugger

5.2 Other Functions

5.2.1 Oscillator Pinout

The oscillators are not mapped to the normal PORT functions and their multiplexing are controlled by registers in the System Controller (SYSCTRL). Refer to !!!CRs_SYSCTRL_Top!!! for more information.

Oscillator	Supply	Signal	I/O Pin
XOSC	VDDIO	XIN	PA14
		XOUT	PA15
XOSC32K	VDDANA	XIN32	PA00
		XOUT32	PA01

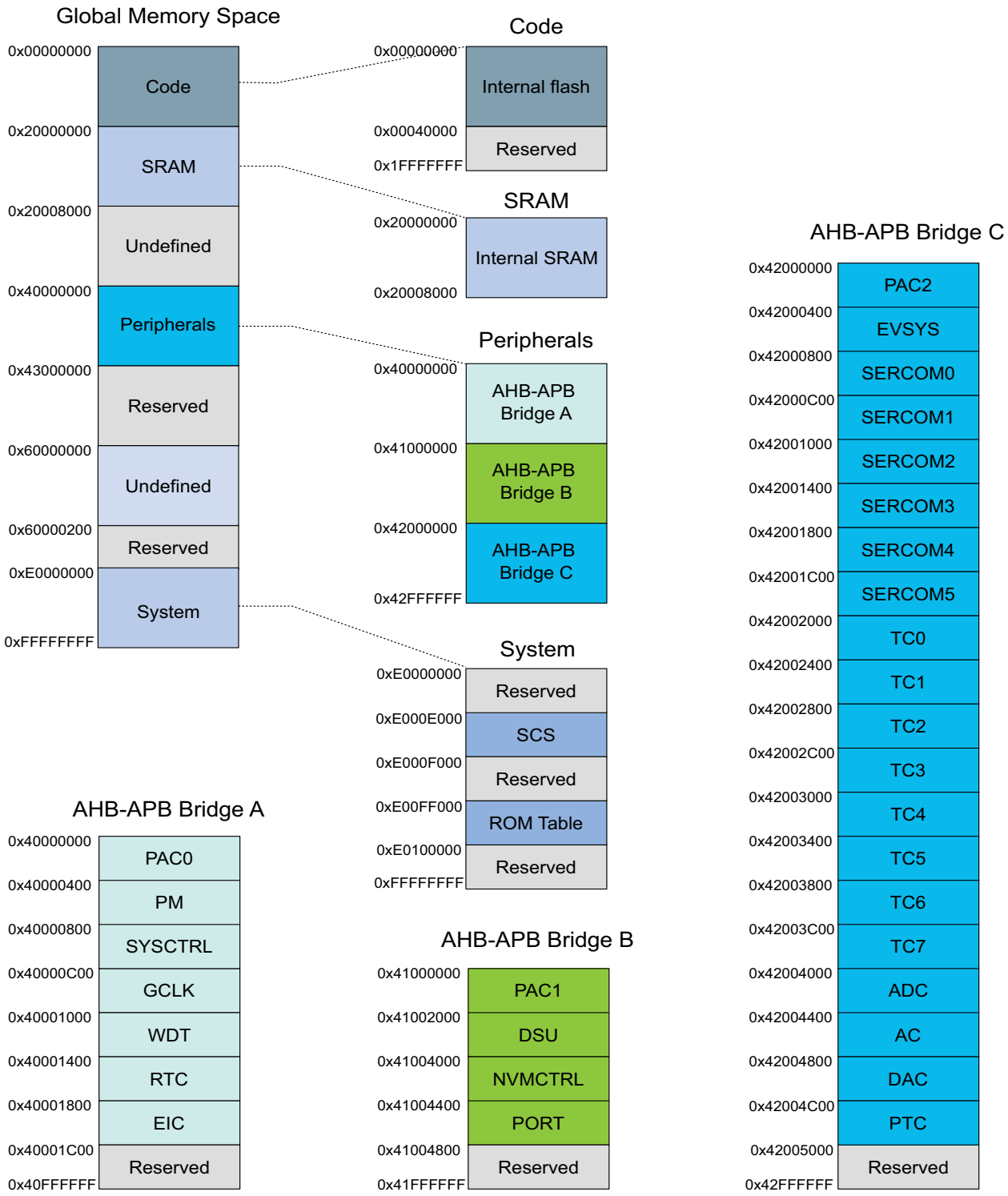
5.2.2 Serial Wire Debug Interface Pinout

After reset, SWCLK functionality is selected for pin PA30 to allow for debugger probe detection. The application software can switch the SWCLK functionality of PA30 to GPIO (or other peripherals) during runtime. PA31, by default, is configured like other normal I/O pins and will automatically switch to SWDIO function when a debugger cold-plugging or hot-plugging is detected. When the device is put in debug mode, application software accesses to PA30 and PA31 PORT registers are ignored.
Refer to !!!CRs_DSU_Top!!! for more information.

Signal	Supply	I/O Pin
SWCLK	VDDIO	PA30
SWDIO	VDDIO	PA31

6. Product Mapping

Figure 6-1. SAM D20 Product Mapping



This figure represents the full configuration of the Atmel® SAM D20 with maximum flash and SRAM capabilities and a full set of peripherals. Refer to the "Configuration Summary" on page 3 for details.

7. Processor and Architecture

7.1 Cortex-M0+ Processor

The Atmel® SAM D20 implements the ARM® Cortex®-M0+ processor, which is based on the ARMv6 architecture and Thumb®-2 ISA. The Cortex M0+ is 100% instruction set compatible with its predecessor, the Cortex-M0 processor, and upward compatible with the Cortex-M3 and Cortex-M4 processors. The ARM Cortex-M0+ implemented is revision r0p1. For more information, refer to www.arm.com.

7.1.1 Cortex-M0+ Configuration

Feature	Configurable Option	SAM D20 Configuration
Interrupts	External interrupts 0-32	32
Data endianness	Little-endian or big-endian	Little-endian
SysTick timer	Present or absent	Present
Number of watchpoint comparators	0, 1, 2	2
Number of breakpoint comparators	0, 1, 2, 3, 4	4
Halting debug support	Present or absent	Present
Multiplier	Fast or small	Fast (single cycle)
Single-cycle I/O port	Present or absent	Present
Wake-up interrupt controller	Supported or not supported	Not supported
Vector Table Offset Register	Present or absent	Present
Unprivileged/Privileged support	Present or absent	Absent
Memory Protection Unit	Not present or 8-region	Not present
Reset all registers	Present or absent	Absent(1)
Instruction fetch width	16-bit only or mostly 32-bit	32-bit

Note: 1. All software run in privileged mode only

The ARM Cortex-M0+ processor has two bus interfaces:

- Single 32-bit AMBA® 3 AHB-Lite™ system interface that provides connections to peripherals and all system memory, including flash and RAM
- Single 32-bit I/O port bus interfacing to the PORT with one-cycle loads and stores

8. Packaging Information

8.1 Thermal Considerations

8.1.1 Thermal Resistance Data

Table 8-1 summarizes the thermal resistance data depending on the package.

Table 8-1. Thermal Resistance Data

Package Type	θ_{JA}	θ_{JC}
32-pin TQFP	68°C/W	25.8°C/W
48-pin TQFP	78.8°C/W	12.3°C/W
64-pin TQFP	66.7°C/W	11.9°C/W
32-pin QFN	37.2°C/W	3.1°C/W
48-pin QFN	33°C/W	11.4°C/W
64-pin QFN	33.5°C/W	11.2°C/W

8.1.2 Junction Temperature

The average chip-junction temperature, T_J, in °C can be obtained from the following equations:

Equation 1

$$T_J = T_A + (P_D \times \theta_{JA})$$

Equation 2

$$T_J = T_A + (P_D \times (\theta_{HEATSINK} + \theta_{JC}))$$

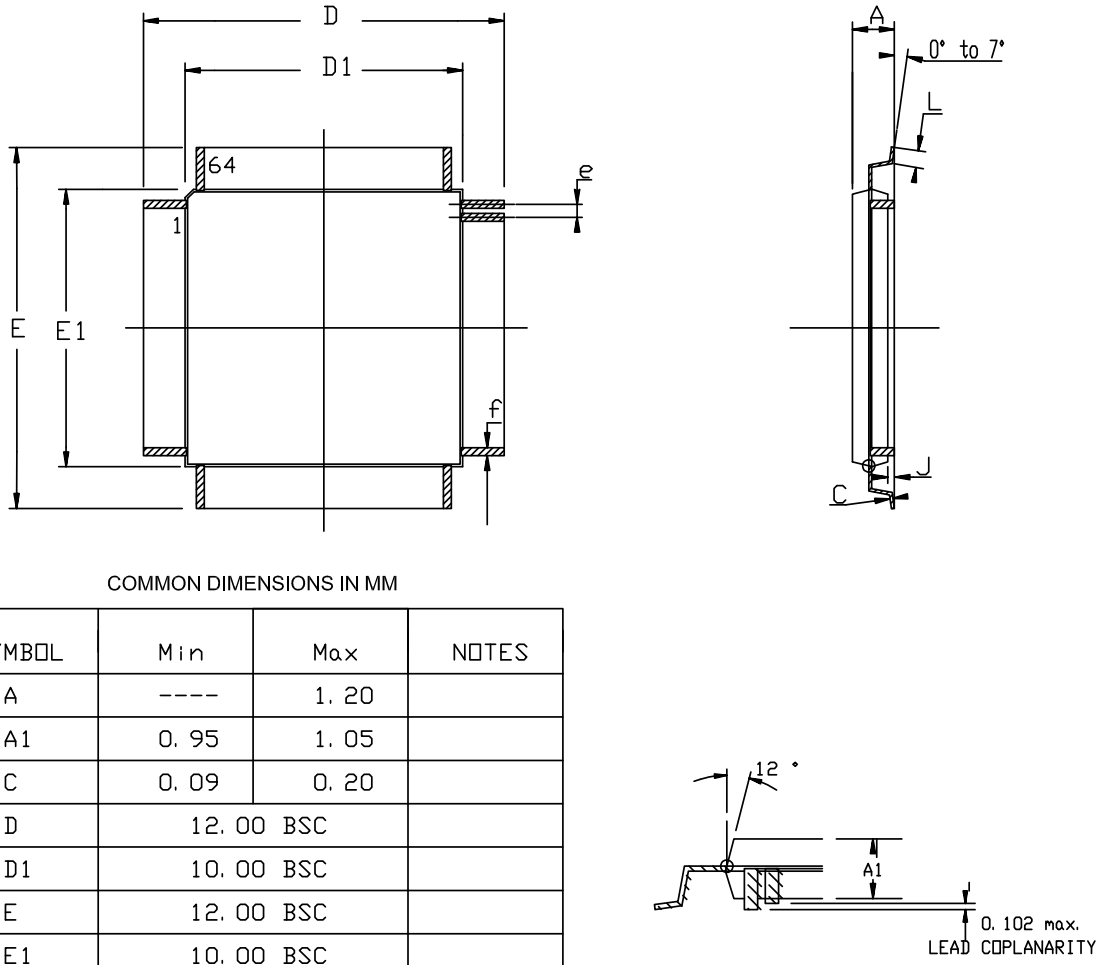
where:

- θ_{JA} = package thermal resistance, Junction-to-ambient (°C/W), provided in Table 8-1
- θ_{JC} = package thermal resistance, Junction-to-case thermal resistance (°C/W), provided in Table 8-1
- $\theta_{HEATSINK}$ = cooling device thermal resistance (°C/W), provided in the manufacturer datasheet
- P_D = device power consumption (W)
- T_A = ambient temperature (°C)

From “Equation 1” , the user can derive the estimated lifetime of the chip and decide if a cooling device is necessary or not. If a cooling device is to be fitted on the chip, “Equation 2” should be used to compute the resulting average chip-junction temperature T_J in °C.

8.2 Package Drawings

8.2.1 64-pin TQFP



COMMON DIMENSIONS IN MM

SYMBOL	Min	Max	NOTES
A	----	1.20	
A1	0.95	1.05	
C	0.09	0.20	
D	12.00 BSC		
D1	10.00 BSC		
E	12.00 BSC		
E1	10.00 BSC		
J	0.05	0.15	
L	0.45	0.75	
e	0.50 BSC		
f	0.17	0.27	

Table 8-2. Device and Package Maximum Weight

300	mg

Table 8-3. Package Characteristics

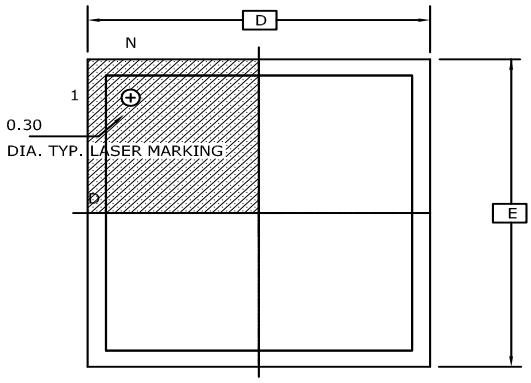
Moisture Sensitivity Level	MSL3

Table 8-4. Package Reference

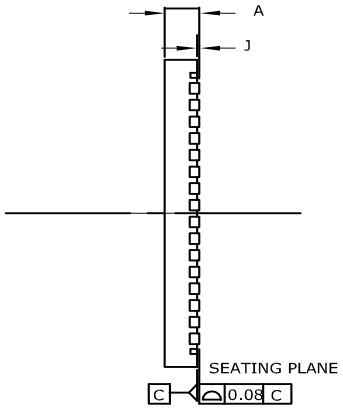
JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

8.2.2 64-pin QFN

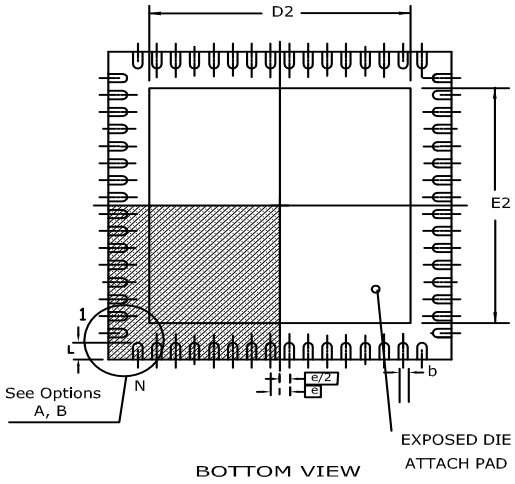
DRAWINGS NOT SCALED



TOP VIEW



SIDE VIEW

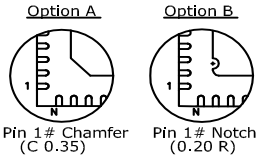


BOTTOM VIEW

COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	-----	1.00	
D/E		9.00 BSC		
D2/E2	4.60	4.70	4.80	
J	0.00	-----	0.05	
b	0.15	0.20	0.25	
e		0.50 BSC		
L	0.30	0.40	0.55	
N		64		



Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MO-220, Variation VMMD-4, for proper dimensions, tolerances, datums, etc.
2. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
If the terminal has the optical radius on the other end of the terminal, the dimension should not be measured in that radius area.

Note: The exposed die attached pad is not connected inside the device.

Table 8-5. Device and Package Maximum Weight

200	mg

Table 8-6. Package Characteristics

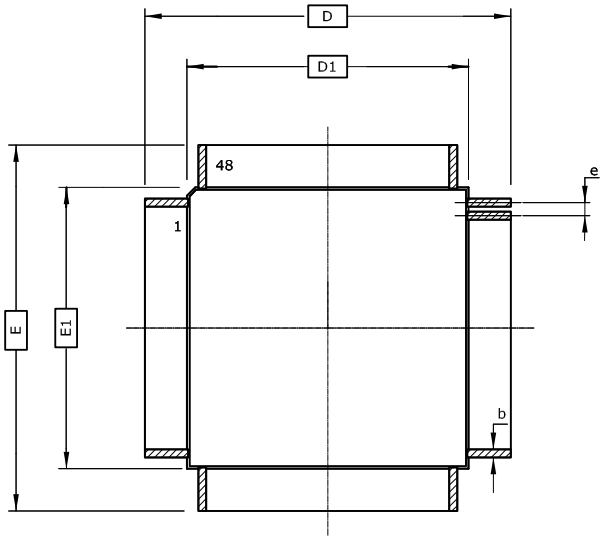
Moisture Sensitivity Level	MSL3

Table 8-7. Package Reference

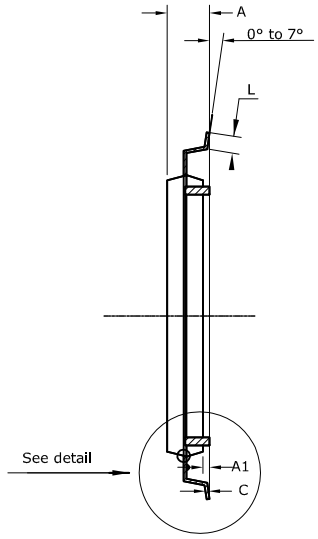
JEDEC Drawing Reference	MO-220
JESD97 Classification	E3

8.2.3 48-pin TQFP

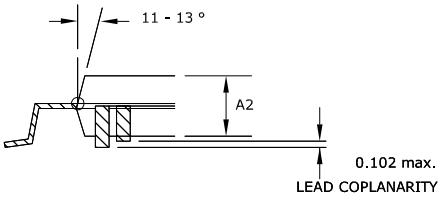
DRAWINGS NOT SCALED



TOP VIEW



SIDE VIEW



DETAIL VIEW

COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-----	-----	1.20	
A1	0.05	-----	0.15	
A2	0.95	-----	1.05	
C	0.09	-----	0.20	
D/E	9.00 BSC			
D1/E1	7.00 BSC			
L	0.45	-----	0.75	
b	0.17	-----	0.27	
e	0.50 BSC			

Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MS-026, Variation ABC.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

Table 8-8. Device and Package Maximum Weight

140	mg

Table 8-9. Package Characteristics

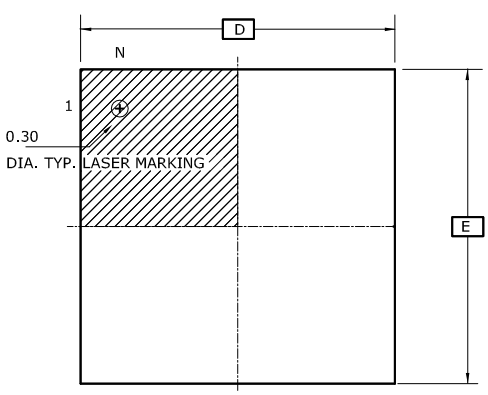
Moisture Sensitivity Level	MSL3

Table 8-10. Package Reference

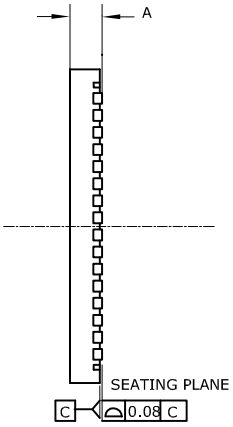
JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

8.2.4 48-pin QFN

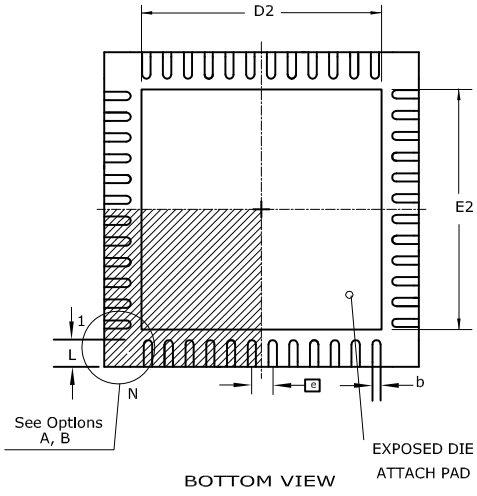
DRAWINGS NOT SCALED



TOP VIEW



SIDE VIEW

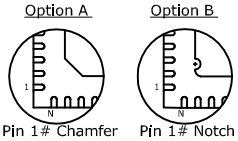


BOTTOM VIEW

COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.85	0.90	
D/E		7.00 BSC		
D2/E2	5.05	5.15	5.25	
b	0.18	0.25	0.30	
e		0.50 BSC		
L	0.30	0.40	0.50	
N		48		



Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MO-220, Variation VKKD-4, for proper dimensions, tolerances, datums, etc.
2. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
If the terminal has the optical radius on the other end of the terminal, the dimension should not be measured in that radius area.

Note: The exposed die attached pad is not connected inside the device.

Table 8-11. Device and Package Maximum Weight

140	mg

Table 8-12. Package Characteristics

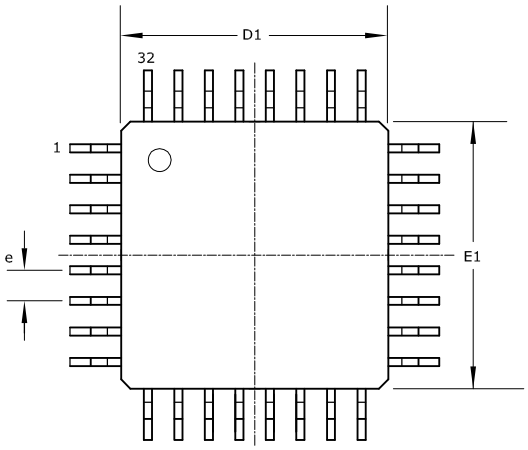
Moisture Sensitivity Level	MSL3

Table 8-13. Package Reference

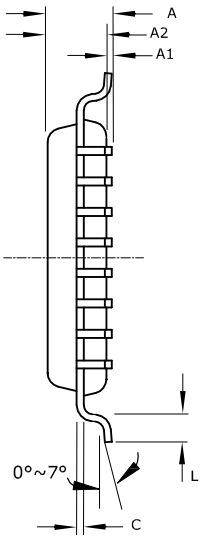
JEDEC Drawing Reference	MO-220
JESD97 Classification	E3

8.2.5 32-pin TQFP

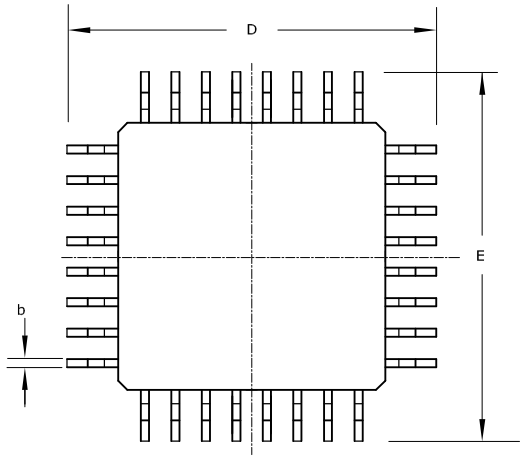
DRAWINGS NOT SCALED



TOP VIEW



SIDE VIEW



BOTTOM VIEW

COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-----	-----	1.20	
A1	0.05	-----	0.15	
A2	0.95	1.00	1.05	
D/E	8.75	9.00	9.25	
D1/E1	6.90	7.00	7.10	2
C	0.09	-----	0.20	
L	0.45	-----	0.75	
b	0.30	-----	0.45	
e	0.80 TYP			
n	32			

Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MS-026, Variation ABA.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

Table 8-14. Device and Package Maximum Weight

100	mg

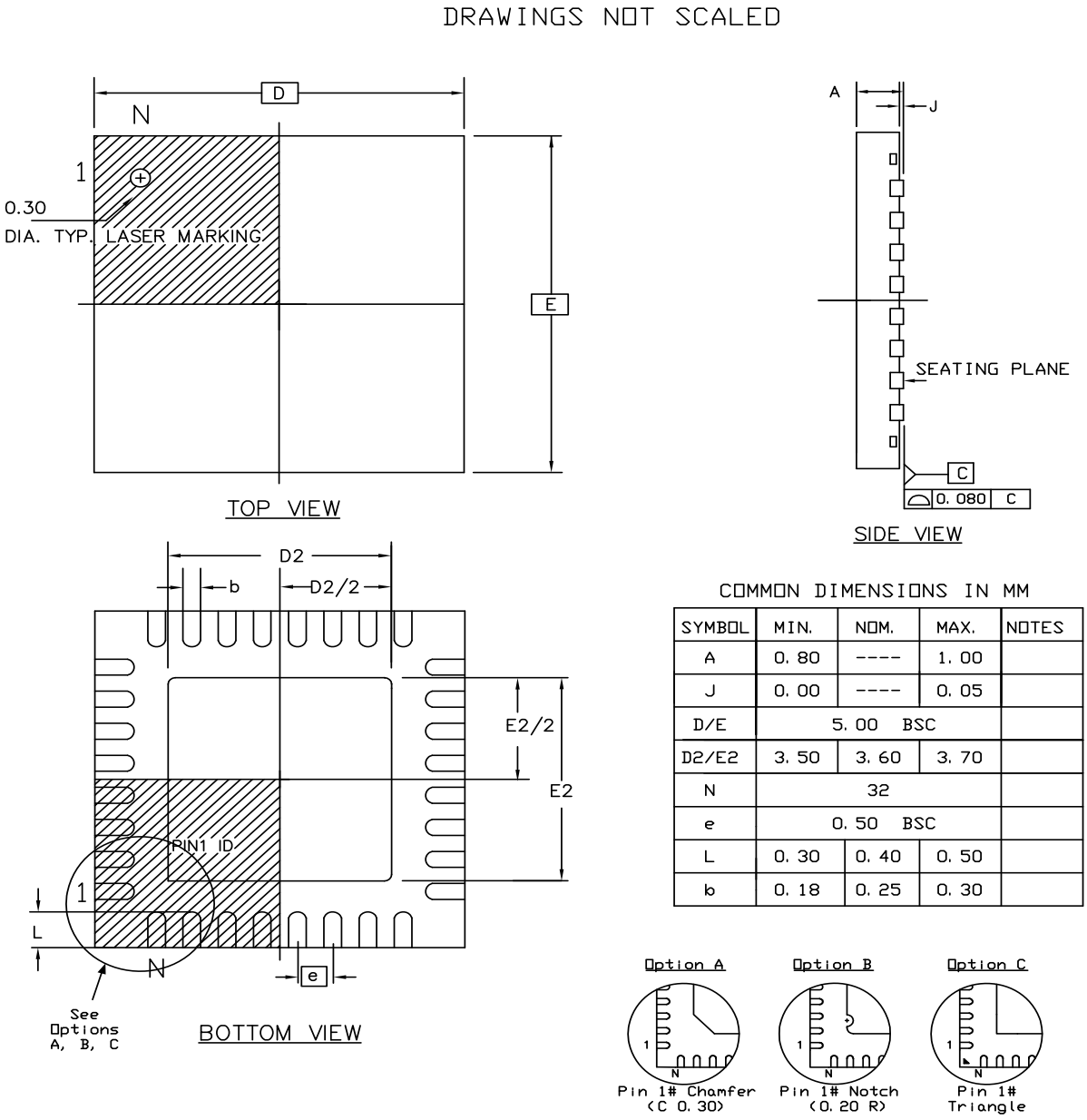
Table 8-15. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 8-16. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

8.2.6 32-pin QFN



SYMBOL	MIN.	NOM.	MAX.	NOTES
A	0.80	----	1.00	
J	0.00	----	0.05	
D/E	5.00 BSC			
D2/E2	3.50	3.60	3.70	
N	32			
e	0.50 BSC			
L	0.30	0.40	0.50	
b	0.18	0.25	0.30	

Note: The exposed die attached pad is connected inside the device to GND and GNDANA connected together.

Table 8-17. Device and Package Maximum Weight

90	mg

Table 8-18. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 8-19. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E3

8.3 Soldering Profile

Table Table 8-20 gives the recommended soldering profile from J-STD-20.

Table 8-20. Soldering Profile

Profile Feature	Green Package
Average Ramp-up Rate (217°C to peak)	3°C/s max.
Preheat Temperature 175°C ±25°C	150-200°C
Time Maintained Above 217°C	60-150s
Time within 5°C of Actual Peak Temperature	30s
Peak Temperature Range	260°C
Ramp-down Rate	6°C/s max
Time 25°C to Peak Temperature	8 minutes max.

A maximum of three reflow passes is allowed per component.

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