

N-channel 600 V, 0.35 Ω typ., 11 A MDmesh II Plus™ low Q_g Power MOSFETs in D²PAK and DPAK packages

Datasheet – production data

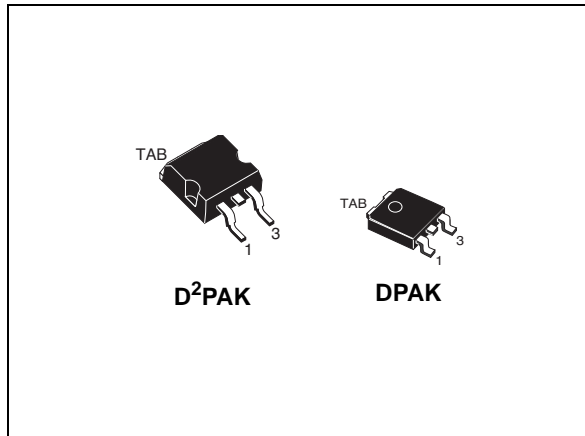
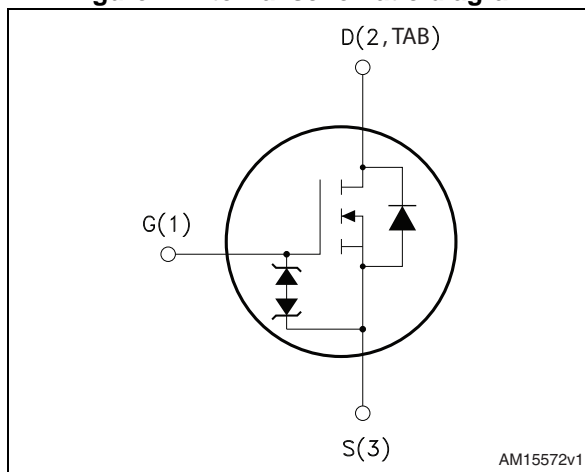


Figure 1. Internal schematic diagram



Features

Order codes	$V_{DS} @ T_{Jmax}$	$R_{DS(on) max}$	I_D
STB13N60M2	650 V	0.38 Ω	11 A
STD13N60M2			

- Extremely low gate charge
- Lower $R_{DS(on)}$ x area vs previous generation
- Low gate input resistance
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs developed using a new generation of MDmesh™ technology: MDmesh II Plus™ low Q_g . These revolutionary Power MOSFETs associate a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. They are therefore suitable for the most demanding high efficiency converters.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STB13N60M2	13N60M2	D ² PAK	Tape and reel
STD13N60M2		DPAK	

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	11	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	7	A
$I_{DM}^{(1)}$	Drain current (pulsed)	44	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	110	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature	- 55 to 150	$^\circ\text{C}$
T_j	Max. operating junction temperature		

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 11\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$; $V_{DS\text{ peak}} < V_{(BR)DSS}$, $V_{DD}=400\text{ V}$.
3. $V_{DS} \leq 480\text{ V}$

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		D ² PAK	DPAK	
$R_{thj-case}$	Thermal resistance junction-case max	1.14		$^\circ\text{C}/\text{W}$
$R_{thj-pcb}$	Thermal resistance junction-pcb max ⁽¹⁾	30	50	$^\circ\text{C}/\text{W}$

1. When mounted on 1 inch² FR-4, 2 Oz copper board

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	2.8	A
E_{AS}	Single pulse avalanche energy (starting $T_j=25\text{ }^\circ\text{C}$, $I_D=I_{AR}$; $V_{DD}=50$)	125	mJ

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	600			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 600\text{ V}$ $V_{DS} = 600\text{ V}$, $T_C = 125\text{ °C}$			1 100	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 25\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 5.5\text{ A}$		0.35	0.38	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	580	-	pF
C_{oss}	Output capacitance		-	32	-	pF
C_{riss}	Reverse transfer capacitance		-	1.1	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }480\text{ V}$, $V_{GS} = 0$	-	120	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	6.6	-	Ω
Q_g	Total gate charge	$V_{DD} = 480\text{ V}$, $I_D = 11\text{ A}$, $V_{GS} = 10\text{ V}$ (see Figure 17)	-	17	-	nC
Q_{gs}	Gate-source charge		-	2.5	-	nC
Q_{gd}	Gate-drain charge		-	9	-	nC

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 5.5\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 16 and 21)	-	11	-	ns
t_r	Rise time		-	10	-	ns
$t_{d(off)}$	Turn-off delay time		-	41	-	ns
t_f	Fall time		-	9.5	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		11	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		44	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 11\text{ A}$, $V_{GS} = 0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 11\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ (see Figure 18)	-	297		ns
Q_{rr}	Reverse recovery charge		-	2.8		μC
I_{RRM}	Reverse recovery current		-	18.5		A
t_{rr}	Reverse recovery time	$I_{SD} = 11\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 18)	-	394		ns
Q_{rr}	Reverse recovery charge		-	3.8		μC
I_{RRM}	Reverse recovery current		-	19		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for D²PAK

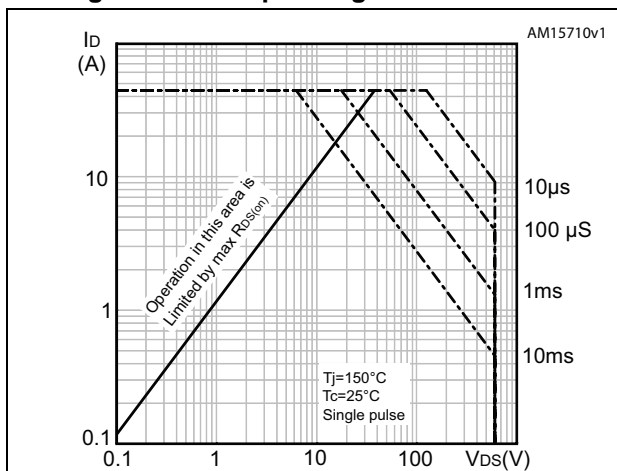


Figure 3. Thermal impedance for D²PAK

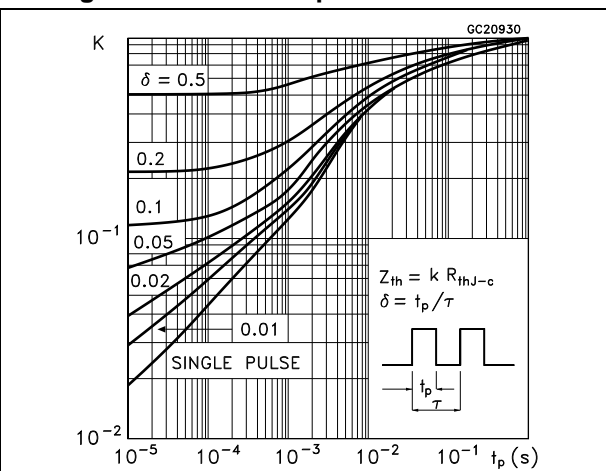


Figure 4. Safe operating area for DPAK

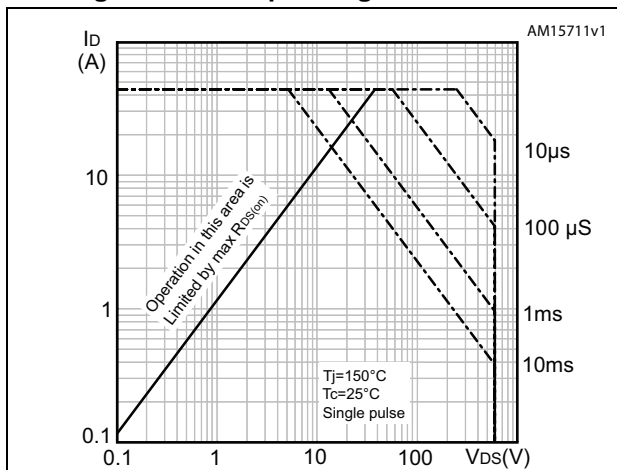


Figure 5. Thermal impedance for DPAK

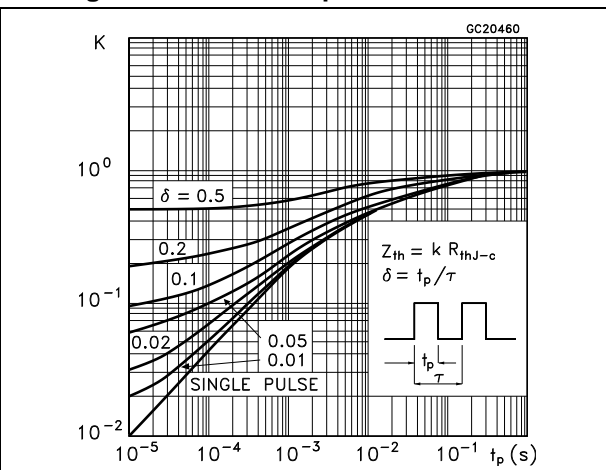


Figure 6. Output characteristics

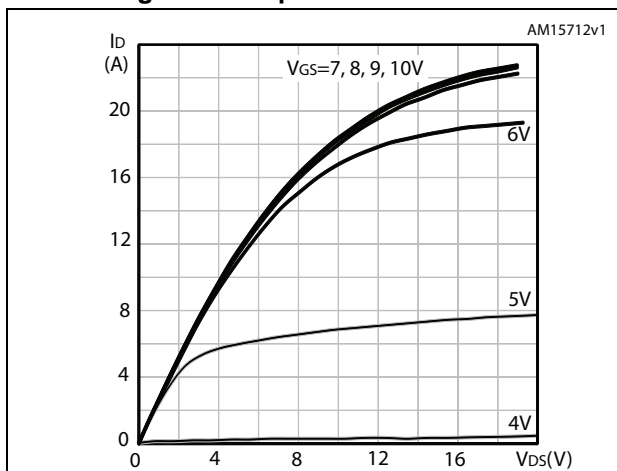


Figure 7. Transfer characteristics

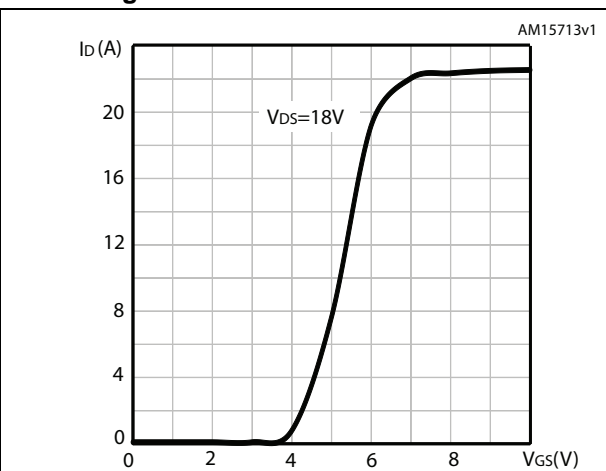


Figure 8. Normalized $V_{(BR)DSS}$ vs temperature

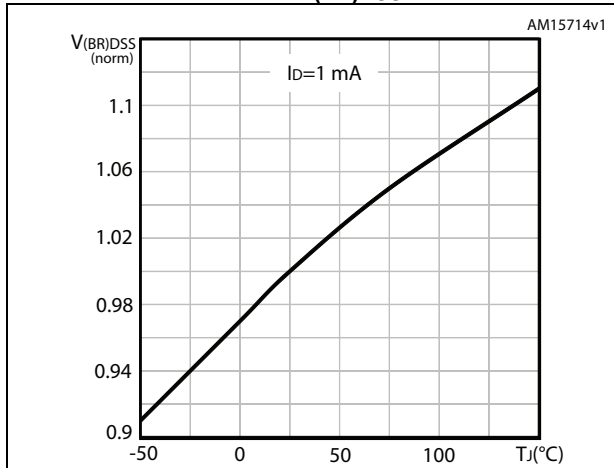


Figure 9. Static drain-source on-resistance

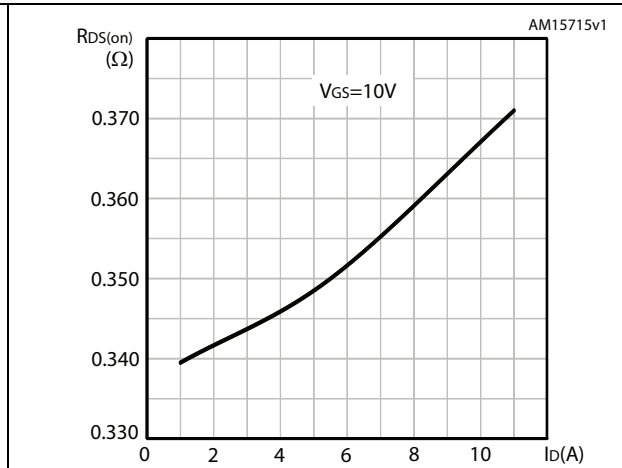


Figure 10. Gate charge vs gate-source voltage

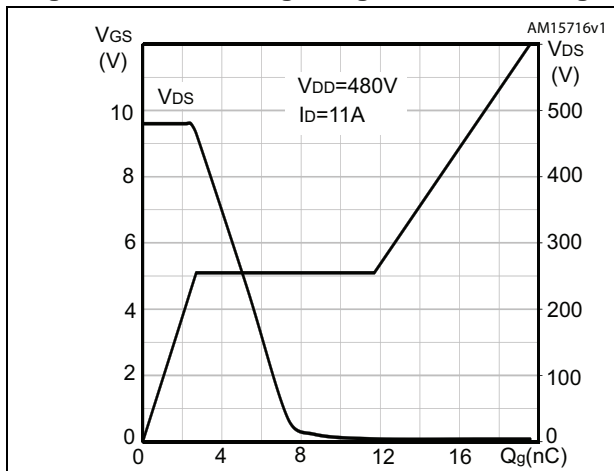


Figure 11. Capacitance variations

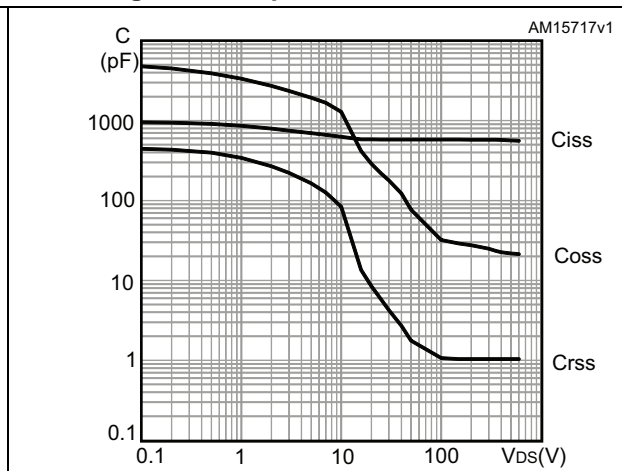


Figure 12. Normalized gate threshold voltage vs temperature

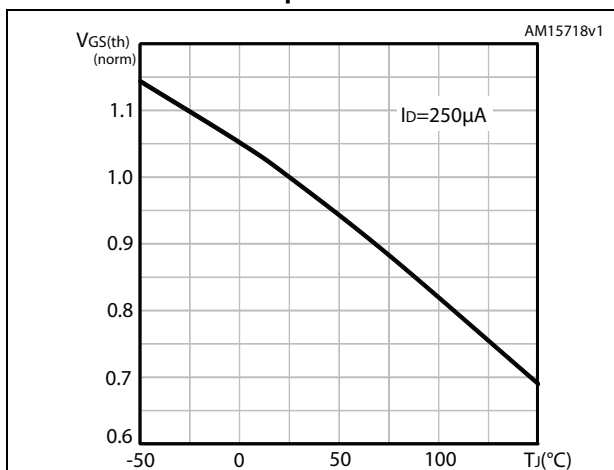


Figure 13. Normalized on-resistance vs temperature

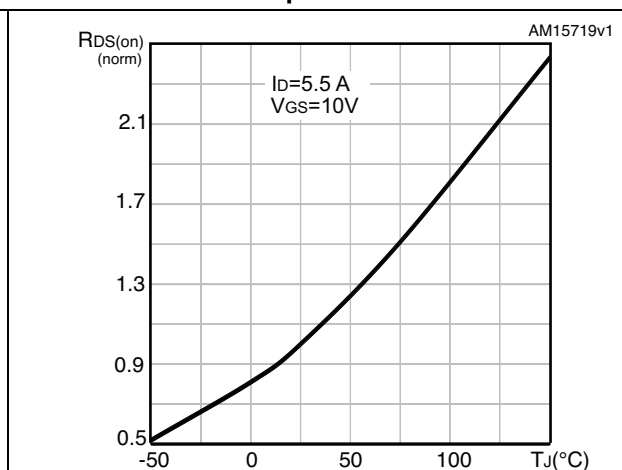


Figure 14. Source-drain diode forward characteristics

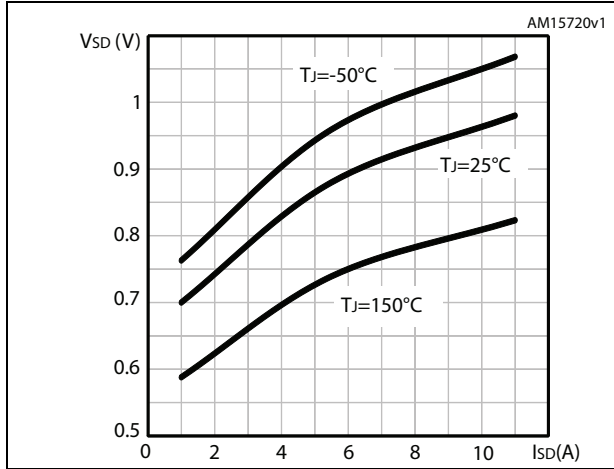
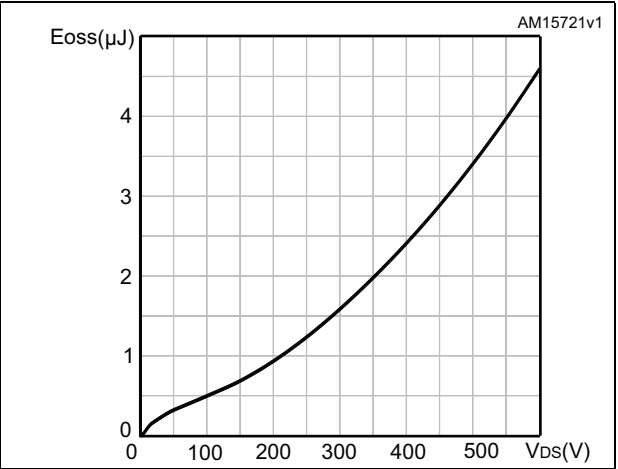


Figure 15. Output capacitance stored energy



3 Test circuits

Figure 16. Switching times test circuit for resistive load



Figure 17. Gate charge test circuit

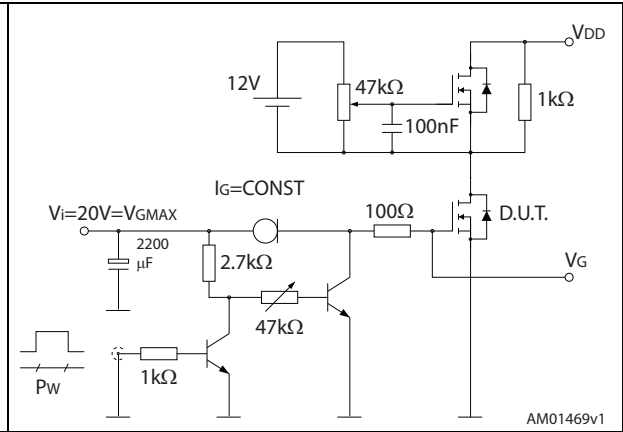


Figure 18. Test circuit for inductive load switching and diode recovery times



Figure 19. Unclamped inductive load test circuit

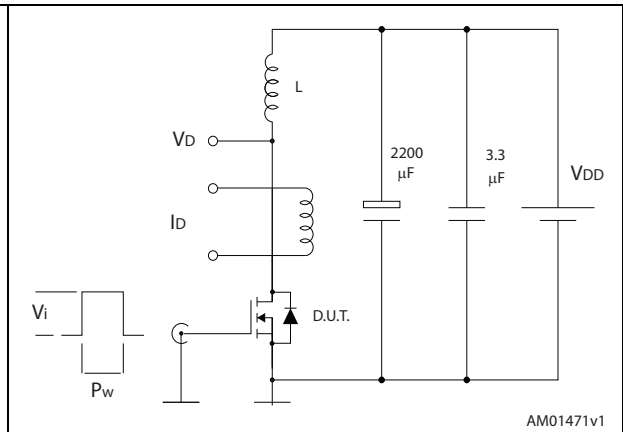


Figure 20. Unclamped inductive waveform

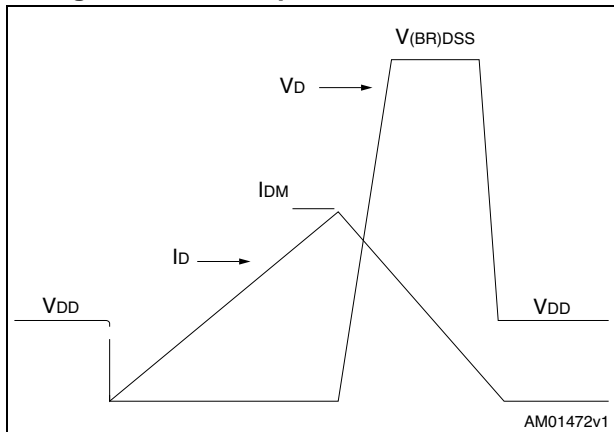
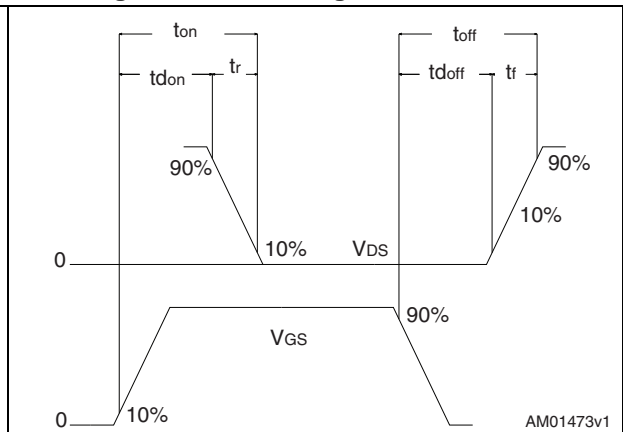


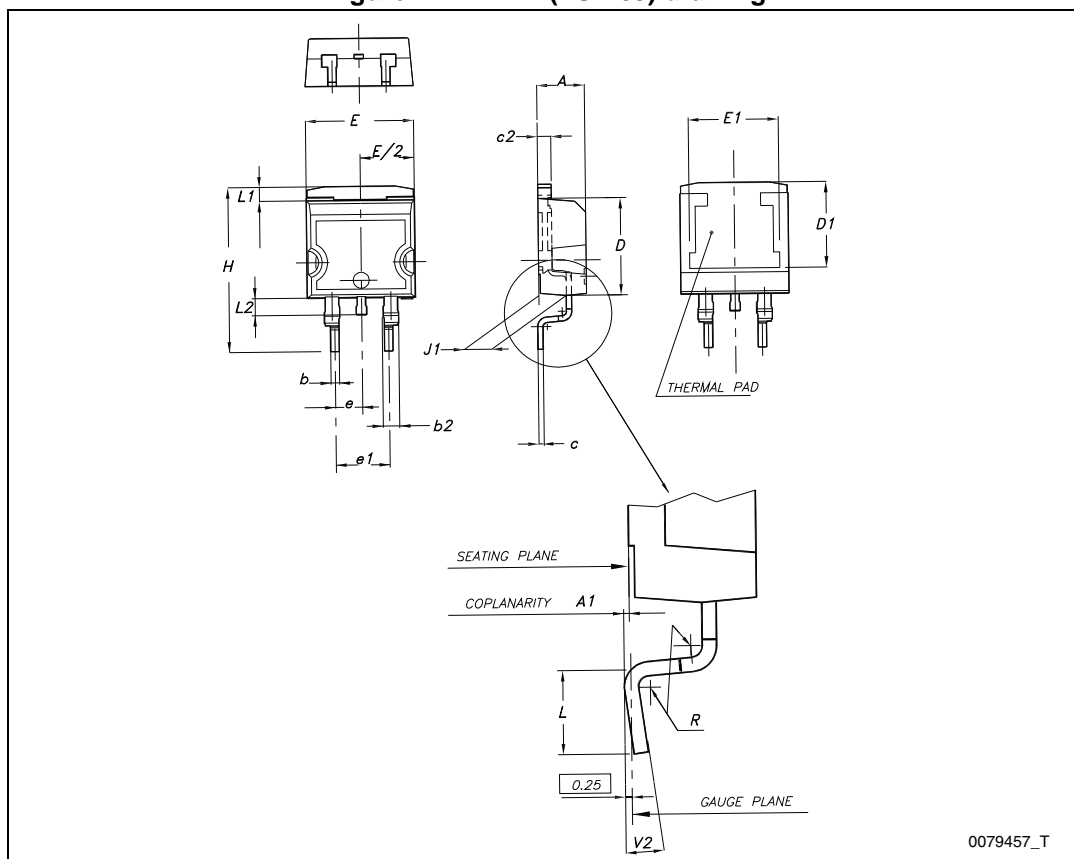
Figure 21. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Figure 22. D²PAK (TO-263) drawing

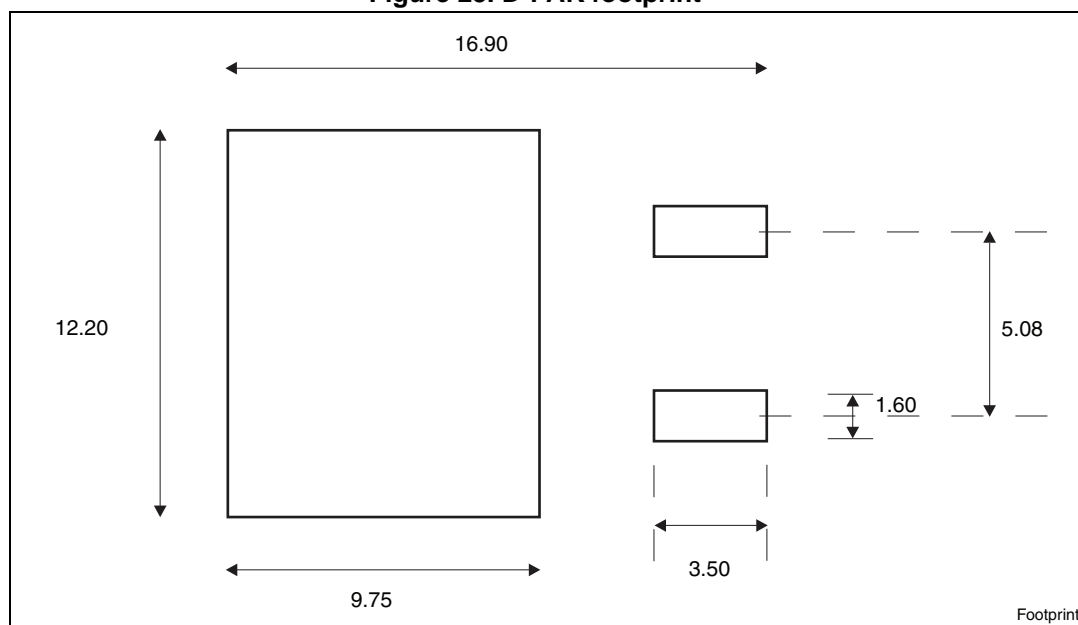


0079457_T

Table 9. D²PAK (TO-263) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50		
E	10		10.40
E1	8.50		
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 23. D²PAK footprint^(a)



a. All dimension are in millimeters

Figure 24. DPAK (TO-252) type A drawing

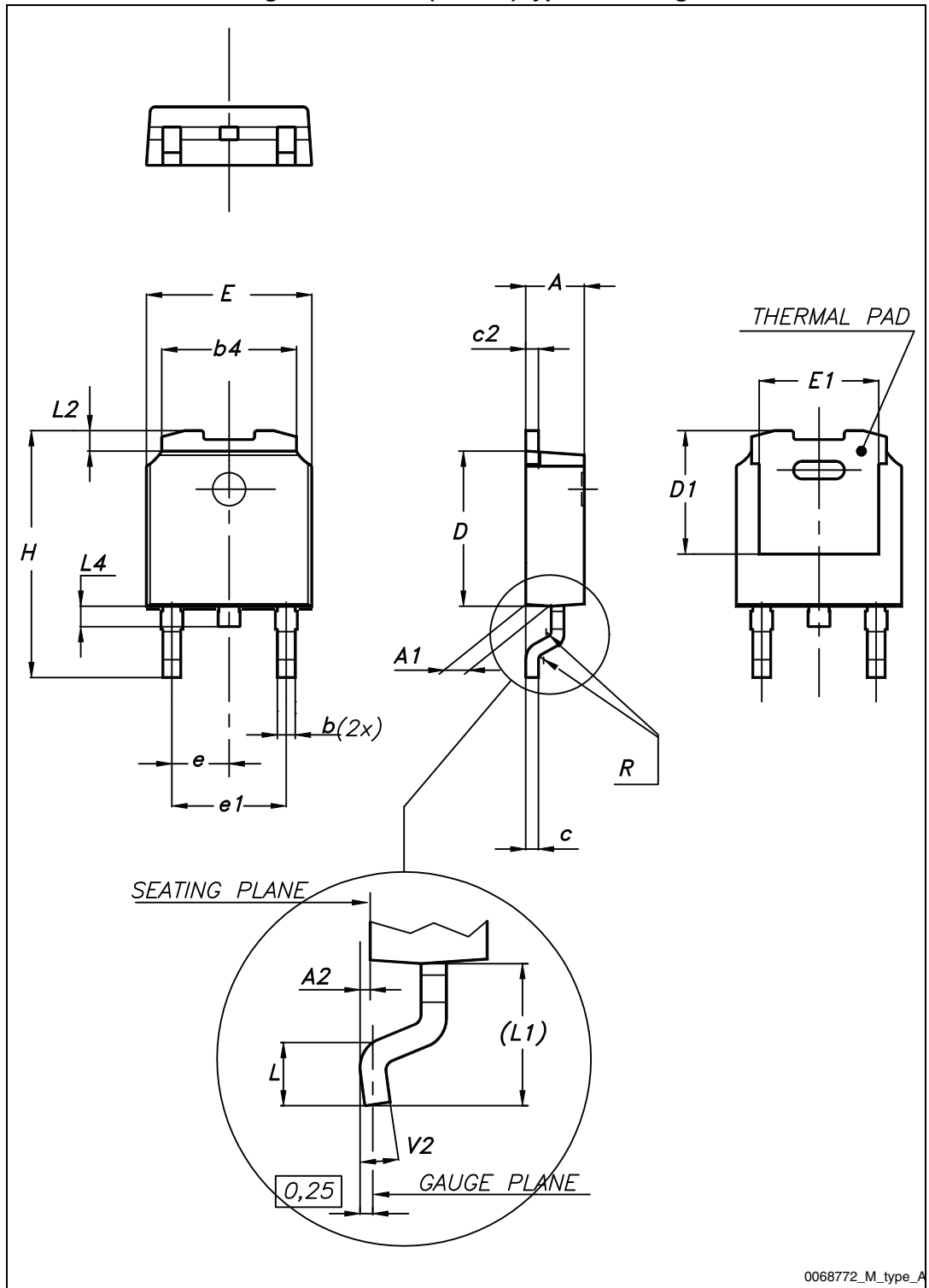
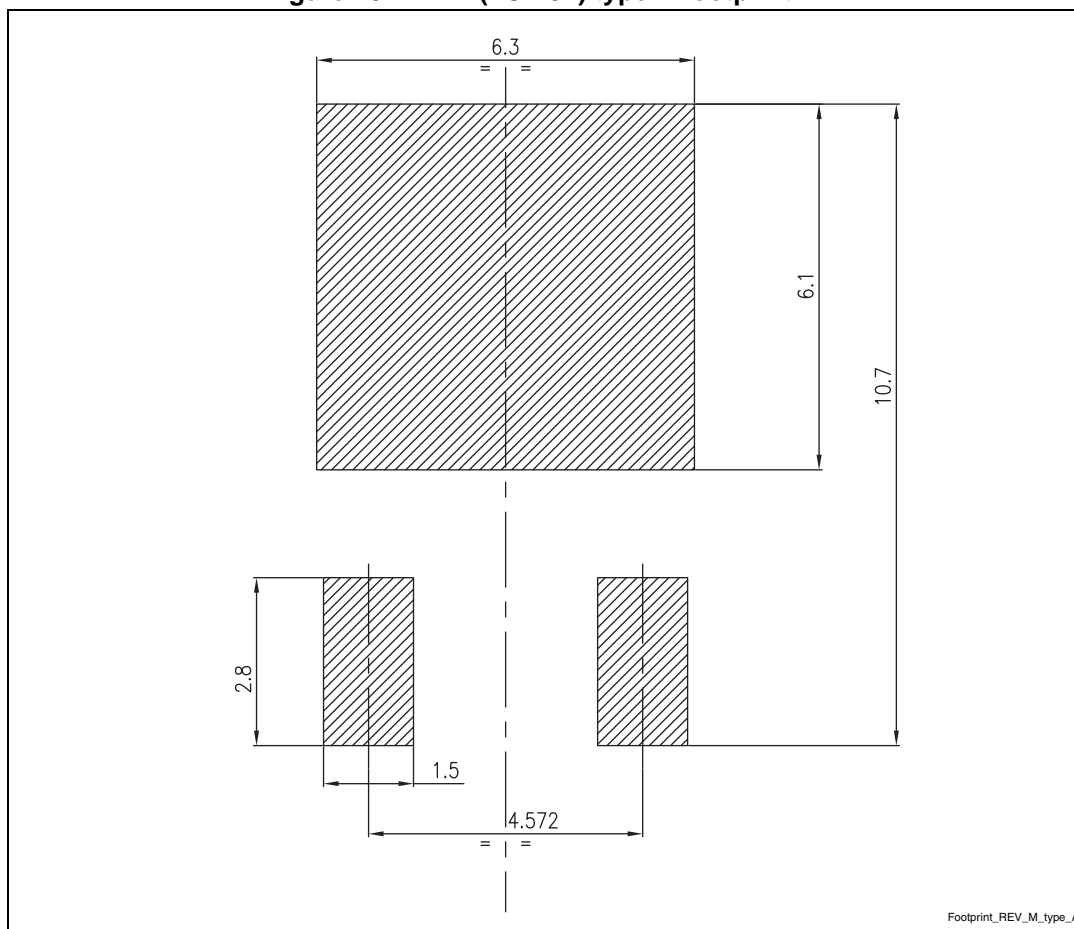


Table 10. DPAK (TO-252) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
(L1)		2.80	
L2		0.80	
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 25. DPAK (TO-252) type A footprint (b)



b. All dimensions are in millimeters

5 Packaging mechanical data

Figure 26. Tape for D²PAK and DPAK (TO-252)

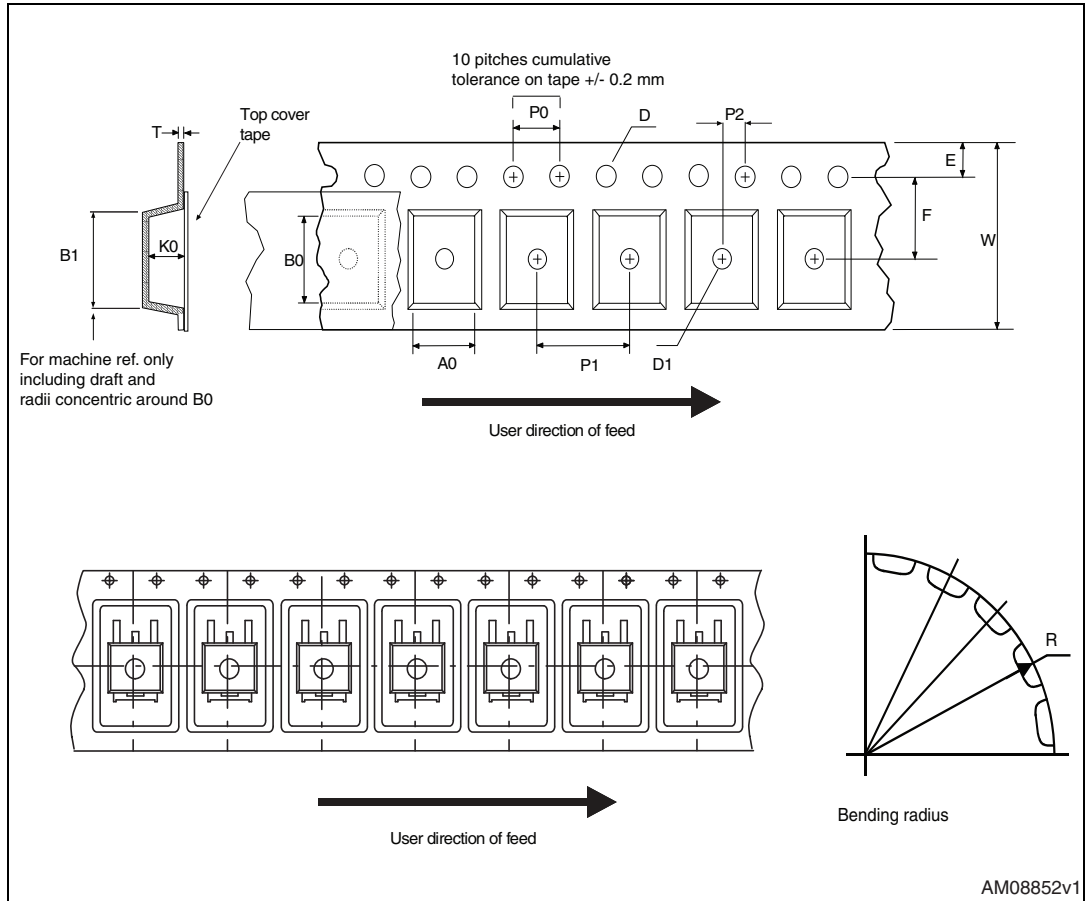


Figure 27. Reel for D²PAK and DPAK

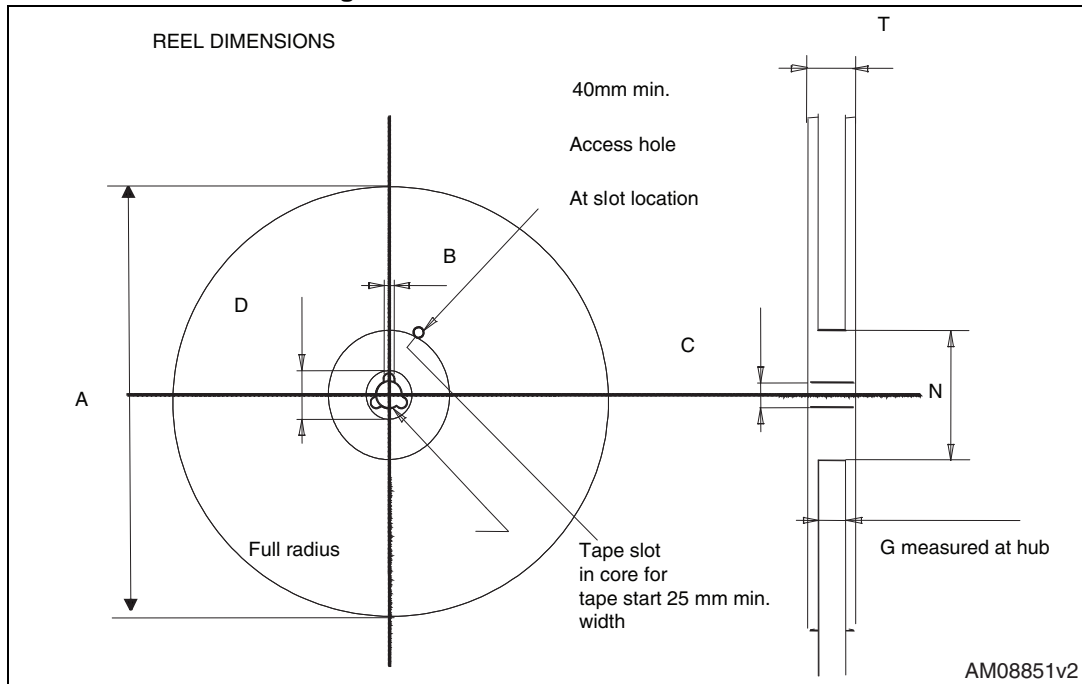


Table 11. D²PAK (TO-263) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1		Base qty	1000
P2	1.9	2.1		Bulk qty	1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Table 12. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

6 Revision history

Table 13. Document revision history

Date	Revision	Changes
22-Apr-2013	1	First release. The part number STD13N60M2 was previously included in datasheet DocID023937
28-Jun-2013	2	<ul style="list-style-type: none">– Document status promoted from preliminary data to production data– Minor text changes
03-Mar-2014	3	<ul style="list-style-type: none">– Updated: Table 10 and Table 25– Minor text changes

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