Rev 1; 9/08

DALLAS SEMICONDUCTOR MAXIM

I²C RTC/Supervisor with Trickle Charger and 512 Bytes EEPROM

DS1388

General Description

The DS1388 I²C real-time clock (RTC), supervisor, and EEPROM is a multifunction device that provides a clock/calendar, programmable watchdog timer, power-supply monitor with reset, and 512 bytes of EEPROM. The clock provides hundredths of seconds, seconds, minutes, and hours, and operates in 24-hour or 12-hour format with an AM/PM indicator. The calendar provides day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. A watchdog timer provides a reset for an unresponsive microprocessor. It is programmable in 10ms intervals from 0.01 to 99.99 seconds. A temperature-compensated voltage reference and comparator circuit monitors the status of V_{CC}. If a primary power failure is detected, the device automatically switches to the backup supply and drives the reset output to the active state. The backup supply maintains time and date operation in the absence of V_{CC}. When V_{CC} returns to nominal levels, the reset is held low for a period to allow the power supply and processor to stabilize. The device also has a pushbutton reset controller, which debounces a reset input signal. The device is accessed through an I²C serial interface.

Applications

Portable Instruments

Point-of-Sale Equipment

Network Interface Cards

Wireless Equipment

Features

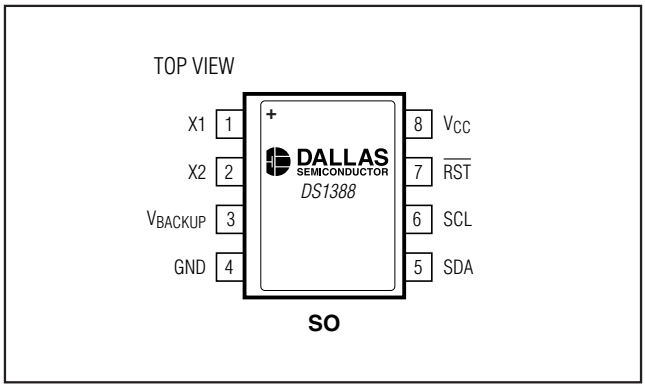
- **Fast (400kHz) I²C Interface**
- **RTC Counts Hundredths of Seconds, Seconds, Minutes, Hours, Day, Date, Month, and Year with Leap Year Compensation Valid Up to 2100**
- **Programmable Watchdog Timer**
- **Automatic Power-Fail Detect and Switch Circuitry**
- **Reset Output with Pushbutton Reset Input Capability**
- **512 x 8 Bits of EEPROM**
- **Integrated Trickle-Charge Capability for Backup Supply**
- **Three Operating Voltages: 5.0V, 3.3V, and 3.0V**
- **Low Timekeeping Voltage Down to 1.3V**
- **-40°C to +85°C Temperature Range**
- **UL Recognized**

Ordering Information

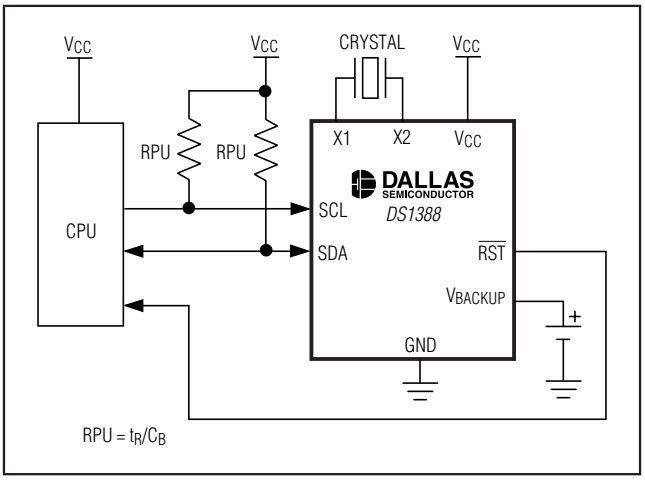
PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
DS1388Z-5+	-40°C to +85°C	8 SO (150 mils)	DS1388-5
DS1388Z-33+	-40°C to +85°C	8 SO (150 mils)	DS138833
DS1388Z-3+	-40°C to +85°C	8 SO (150 mils)	DS1388-3

+Denotes a lead-free/RoHS-compliant package.

Pin Configuration



Typical Operating Circuit



I²C RTC/Supervisor with Trickle Charger and 512 Bytes EEPROM

ABSOLUTE MAXIMUM RATINGS

Voltage Range on V_{CC} Pin Relative to Ground .....-0.3V to +6.0V
Voltage Range on Inputs Relative to Ground .....-0.3V to (V_{CC} + 0.3V)
Operating Temperature Range (noncondensing) .....-40°C to +85°C
Storage Temperature Range .....-55°C to +125°C
Soldering Temperature.....Refer to the IPC/JEDEC J-STD-020 Specification.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = -40°C to +85°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	(Note 2)	DS1388Z-5	4.5	5	5.5	V
			DS1388Z-33	2.97	3.3	3.63	
			DS1388Z-3	2.7	3	3.3	
Logic 1	V_{IH}	(Note 2)		0.7 x V_{CC}		V_{CC} + 0.3	V
Logic 0	V_{IL}	(Note 2)		-0.3		+0.3 x V_{CC}	V
Pullup Voltage (SCL, SDA), V_{CC} = 0V	V_{PU}					5.5	V
V_{BACKUP} Voltage	V_{BACKUP}	(Note 2)		1.3	3.0	5.5	V
Power-Fail Voltage	V_{PF}	(Note 2)	DS1388Z-5	4.15	4.33	4.50	V
			DS1388Z-33	2.70	2.88	2.97	
			DS1388Z-3	2.45	2.60	2.70	

DC ELECTRICAL CHARACTERISTICS

(**V_{CC} = $V_{CC(MIN)}$ to $V_{CC(MAX)}$**, T_A = -40°C to +85°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Trickle-Charger Current-Limiting Resistors	R1	(Notes 3, 4)		250		Ω
	R2	(Note 5)		2000		
	R3	(Note 6)		4000		
Input Leakage (SCL)	I_{LI}		-1		+1	µA
I/O Leakage (SDA)	I_{LO}		-1		+1	µA
I/O Leakage ($\overline{RST}$)	I_{LORST}	(Note 7)	-200		+10	µA
SDA Logic 0 Output (V_{OL} = 0.15 x V_{CC})	I_{OLDOUT}				3	mA

DC ELECTRICAL CHARACTERISTICS (continued)

(**V_{CC} = $V_{CC(MIN)}$ to $V_{CC(MAX)}$**, T_A = -40°C to +85°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{RST}$ Logic 0 Output	I_{OLSIR}	V_{CC} > 2V; V_{OL} = 0.4V				3.0	mA
		1.8V < V_{CC} < 2V; V_{OL} = 0.2 x V_{CC}				3.0	
		1.3V < V_{CC} < 1.8V; V_{OL} = 0.2 x V_{CC}				250	µA
V_{CC} Active Current, EEPROM Read, I^2C Read/Write Access	I_{CCER}	(Note 8)	DS1388Z-5			600	µA
			DS1388Z-33			250	
			DS1388Z-3			225	
V_{CC} Active Current, EEPROM Write Cycle	I_{CCEW}	(Note 8)	DS1388Z-5			1.0	mA
			DS1388Z-33			0.70	
			DS1388Z-3			0.65	
V_{CC} Standby Current	I_{CCS}	(Note 9)	DS1388Z-5			270	µA
			DS1388Z-33		100	150	
			DS1388Z-3			140	
V_{BACKUP} Leakage Current (V_{BACKUP} = 3.7V, V_{CC} = $V_{CC(MAX)}$)	$I_{BACKUPLKG}$				15	100	nA
EEPROM Write/Erase Cycles	t_{WR}	T_A = +25°C (guaranteed by design)		200k			Cycles
		T_A = -40°C to +85°C (guaranteed by design)		50k			

DC ELECTRICAL CHARACTERISTICS

(**V_{CC} = 0V, V_{BACKUP} = 3.7V**, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{BACKUP} Current, OSC On ($\overline{EOSC}$ = 0), SDA = SCL = 0V	I_{BACKUP}	(Note 10)		410	550	nA
V_{BACKUP} Current, OSC Off ($\overline{EOSC}$ = 1), SDA = SCL = 0V (Data Retention)	$I_{BACKUPDR}$	(Note 10)		10	100	nA

I²C RTC/Supervisor with Trickle Charger and 512 Bytes EEPROM

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = $V_{CC(MIN)}$ to $V_{CC(MAX)}$, T_A = -40°C to +85°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	Fast mode	100		400	kHz
		Standard mode	0		100	
Bus Free Time Between a STOP and START Condition	t_{BUF}	Fast mode	1.3			µs
		Standard mode	4.7			
Hold Time (Repeated) START Condition (Note 11)	$t_{HD:STA}$	Fast mode	0.6			µs
		Standard mode	4.0			
LOW Period of SCL Clock	t_{LOW}	Fast mode	1.3			µs
		Standard mode	4.7			
HIGH Period of SCL Clock	t_{HIGH}	Fast mode	0.6			µs
		Standard mode	4.0			
Setup Time for a Repeated START Condition	$t_{SU:STA}$	Fast mode	0.6			µs
		Standard mode	4.7			
Data Hold Time (Notes 12, 13)	$t_{HD:DAT}$	Fast mode	0		0.9	µs
		Standard mode	0			
Data Setup Time (Note 14)	$t_{SU:DAT}$	Fast mode	100			ns
		Standard mode	250			
Rise Time of Both SDA and SCL Signals (Note 15)	t_R	Fast mode	20 + $0.1C_B$		300	ns
		Standard mode			1000	
Fall Time of Both SDA and SCL Signals (Note 15)	t_F	Fast mode	20 + $0.1C_B$		300	ns
		Standard mode			300	
Setup Time for STOP Condition	$t_{SU:STO}$	Fast mode	0.6			µs
		Standard mode	4.0			
Capacitive Load for Each Bus Line (Note 15)	C_B				400	pF
I/O Capacitance (SDA, SCL, $\overline{RST}$)	$C_{I/O}$	+25°C			10	pF
Pushbutton Debounce	PB_{DB}			160	180	ms
Reset Active Time	t_{RST}			160	180	ms
EEPROM Write Cycle Time	t_{WEE}			8	10	ms
Oscillator Stop Flag (OSF) Delay (Note 16)	t_{OSF}			20		ms

POWER-UP/POWER-DOWN CHARACTERISTICS

(T_A = -40°C to +85°C) (Note 1) (Figures 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Detect to Recognize Inputs (V_{CC} Rising)	t_{RST}	(Note 17)		160	180	ms
V_{CC} Fall Time; $V_{PF(MAX)}$ to $V_{PF(MIN)}$	t_F		300			µs
V_{CC} Rise Time; $V_{PF(MIN)}$ to $V_{PF(MAX)}$	t_R		0			µs

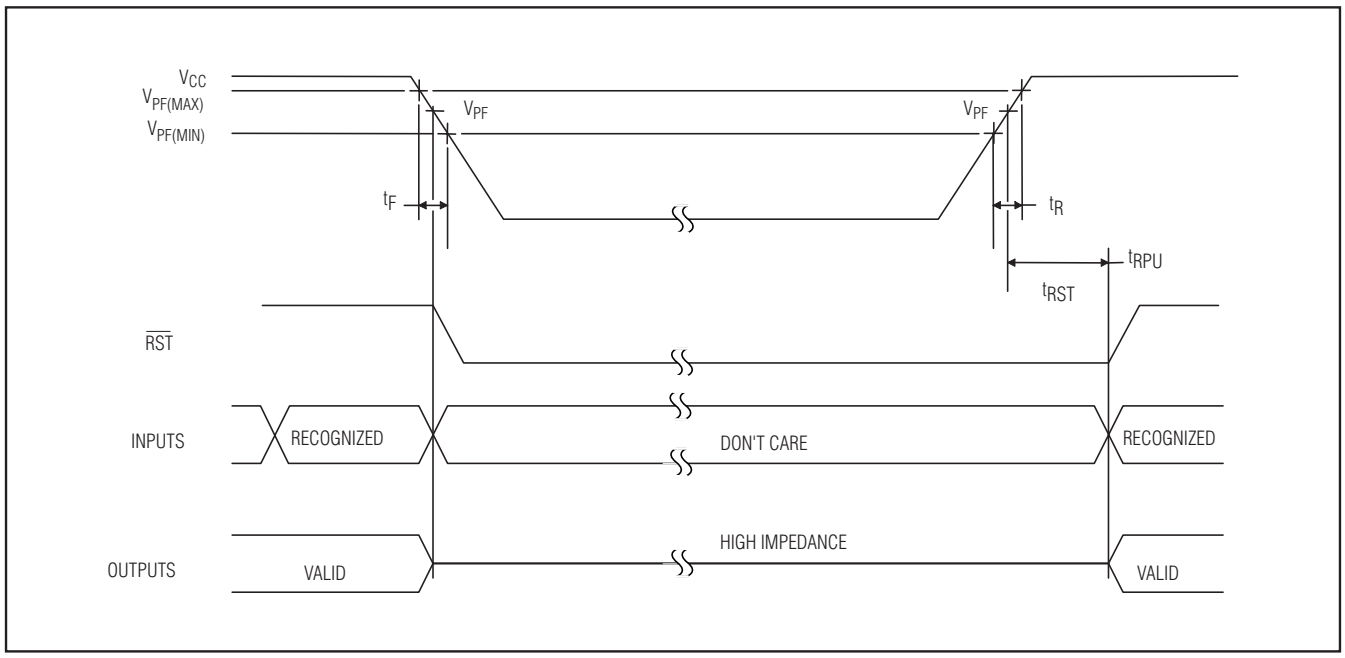


Figure 1. Power-Up/Down Timing

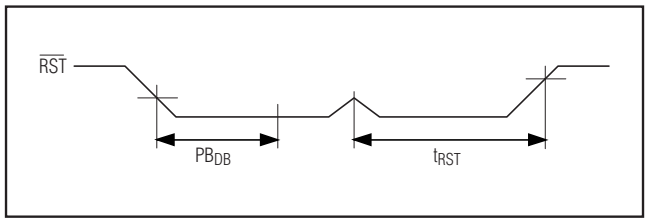


Figure 2. Pushbutton Reset Timing

I²C RTC/Supervisor with Trickle Charger and 512 Bytes EEPROM

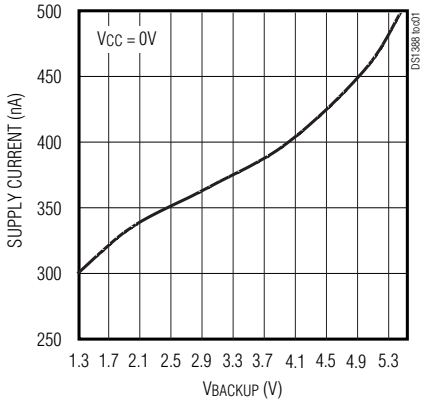
WARNING: Under no circumstances are negative undershoots, of any amplitude, allowed when device is in write protection.

Note 1: Limits at -40°C are guaranteed by design and are not production tested.
Note 2: All voltages are referenced to ground.
Note 3: Measured at V_{CC} = typ, V_{BACKUP} = 0V, register 0Ah, block 0h = A5h.
Note 4: The use of the 250Ω trickle-charge resistor is not allowed at V_{CC} > 3.63V and should not be enabled.
Note 5: Measured at V_{CC} = typ, V_{BACKUP} = 0V, register 0Ah, block 0h = A6h.
Note 6: Measured at V_{CC} = typ, V_{BACKUP} = 0V, register 0Ah, block 0h = A7h.
Note 7: The $\overline{RST}$ pin has an internal 50kΩ pullup resistor to V_{CC}.
Note 8: I_{CCA}—SCL clocking at max frequency = 400kHz.
Note 9: Specified with I²C bus inactive.
Note 10: Measured with a 32.768kHz crystal attached to X1 and X2.
Note 11: After this period, the first clock pulse is generated.
Note 12: A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IHMIN} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
Note 13: The maximum $t_{HD:DAT}$ need only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
Note 14: A fast-mode device can be used in a standard-mode system, but the requirement $t_{SU:DAT} \geq 250ns$ must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{R(MAX)} + t_{SU:DAT} = 1000 + 250 = 1250ns$ before the SCL line is released.
Note 15: C_B—total capacitance of one bus line in pF.
Note 16: The parameter t_{OSF} is the period of time that the oscillator must be stopped for the OSF flag to be set over the voltage range of $0V \leq V_{CC} \leq V_{CC(MAX)}$ and $1.3V \leq V_{BACKUP} \leq 3.7V$.
Note 17: If the oscillator is disabled or stopped, $\overline{RST}$ goes inactive after t_{RST} plus the startup time of the oscillator.

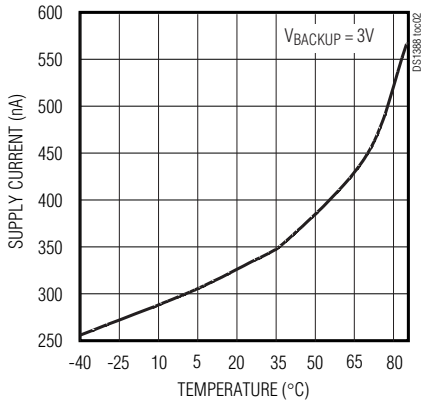
Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

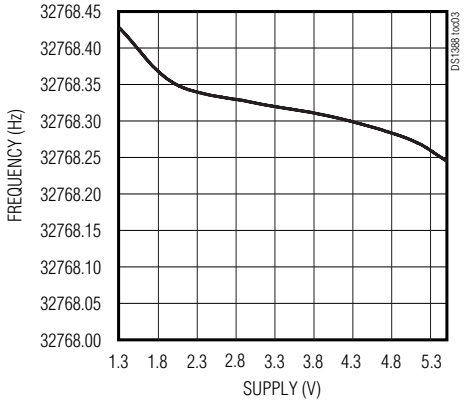
IBACKUP SUPPLY CURRENT VOLTAGE vs. VBACKUP



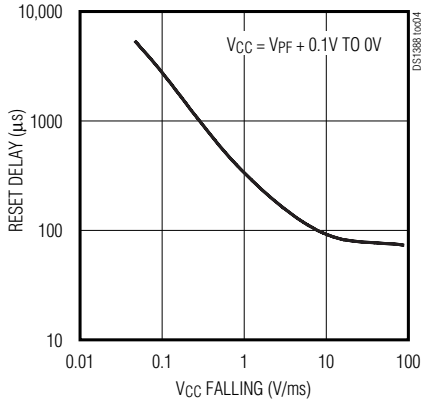
IBACKUP SUPPLY CURRENT VOLTAGE vs. TEMPERATURE



OSCILLATOR FREQUENCY vs. SUPPLY VOLTAGE



VCC FALLING vs. $\overline{RST}$ DELAY

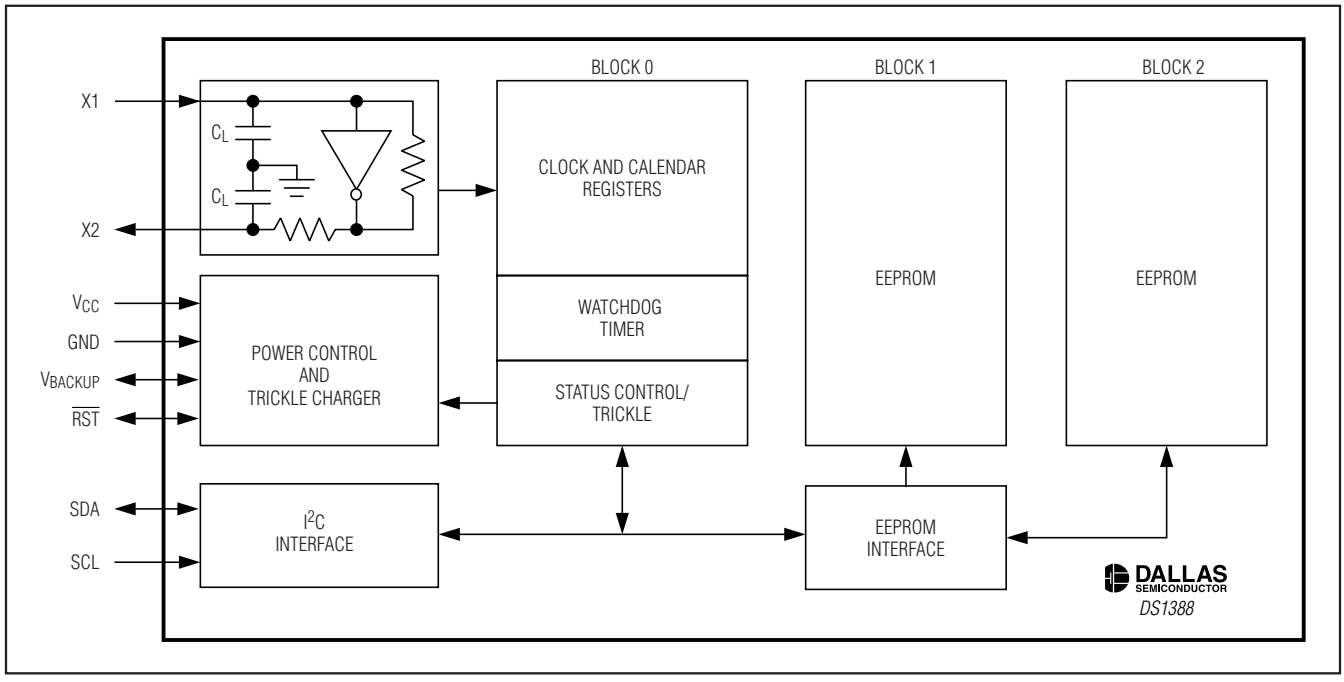


I²C RTC/Supervisor with Trickle Charger and 512 Bytes EEPROM

Pin Description

PIN	NAME	FUNCTION
1	X1	Connections for a Standard 32.768kHz Quartz Crystal. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (C_L) of 6.0pF. Pin X1 is the input to the oscillator and can optionally be connected to an external 32.768kHz oscillator. The output of the internal oscillator, pin X2, is floated if an external oscillator is connected to pin X1.
2	X1	
3	V_{BACKUP}	Connection for a Secondary Power Supply. Supply voltage must be held between 1.3V and 5.5V for proper operation. This pin can be connected to a primary cell, such as a lithium button cell. Additionally, this pin can be connected to a rechargeable cell or a super cap when used with the trickle-charge feature. If not used, this pin must be connected to ground. UL recognized to ensure against reverse charging current when used with a lithium battery (www.maxim-ic.com/qa/info/ul/).
4	GND	Ground
5	SDA	Serial Data Output. SDA is the input/output for the I²C serial interface. This pin is open drain and requires an external pullup resistor. The pullup voltage can be up to 5.5V, regardless of the voltage on V_{CC}.
6	SCL	Serial Clock Input. SCL is the clock input for the I²C interface and is used to synchronize data movement on the serial interface. Up to 5.5V can be used for this pin, regardless of the voltage on V_{CC}.
7	$\overline{RST}$	Active-Low, Open-Drain Reset Output. This pin indicates the status of V_{CC} relative to the V_{PF} specification. As V_{CC} falls below V_{PF}, the $\overline{RST}$ pin is driven low. When V_{CC} exceeds V_{PF}, for t_{RST}, the $\overline{RST}$ pin is driven high impedance. The active-low, open-drain output is combined with a debounced pushbutton input function. This pin can be activated by a pushbutton reset request. It has an internal 50kΩ nominal value pullup resistor to V_{CC}. No external pullup resistors should be connected. If the crystal oscillator is disabled, the startup time of the oscillator is added to the t_{RST} delay.
8	V_{CC}	DC Power Pin for Primary Power Supply

Block Diagram



Detailed Description

The DS1388 I²C RTC, supervisor, and EEPROM is a multifunction device that provides a clock/calendar, programmable watchdog timer, power-supply monitor with reset, and 512 bytes of EEPROM. The clock provides hundredths of seconds, seconds, minutes, and hours, and operates in 24-hour or 12-hour format with an AM/PM indicator. The calendar provides day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. A watchdog timer provides a reset for an unresponsive microprocessor. It is programmable in 10ms intervals from 0.01 to 99.99 seconds. A temperature-compensated voltage reference and comparator circuit monitors the status of V_{CC}. If a primary power failure is detected, the device automatically switches to the backup supply and drives the reset output to the active state. When V_{CC} returns to nominal levels, the reset is held low for a period to allow the power supply and processor to stabilize. The device also has a pushbutton reset controller, which debounces a reset input signal. The device is accessed through an I²C serial interface.

Operation

The DS1388 operates as a slave device on the I²C bus. Access is obtained by implementing a START condition and providing a device identification code followed by data. Subsequent registers can be accessed sequentially until a STOP condition is executed. See the *Block Diagram*, which shows the main elements of the serial real-time clock.

Power Control

The power-control function is provided by a precise, temperature-compensated voltage reference and a comparator circuit that monitors the V_{CC} level. The device is fully accessible and data can be written and read when V_{CC} is greater than V_{PF}. However, when V_{CC} falls below V_{PF}, the internal clock registers are blocked from any access. If V_{PF} is less than V_{BACKUP}, the device power is switched from V_{CC} to V_{BACKUP} when V_{CC} drops below V_{PF}. If V_{PF} is greater than V_{BACKUP}, the device power is switched from V_{CC} to V_{BACKUP} when V_{CC} drops below V_{BACKUP}. The registers are maintained from the V_{BACKUP} source until V_{CC} is returned to nominal levels (Table 1). After V_{CC} returns above V_{PF}, read and write access is allowed after $\overline{RST}$ goes high (Figure 1).

On first application of power to the device, the time and date registers are reset to 01/01/00 01 00:00:00 (MM/DD/YY DOW HH:MM:SS).

Table 1. Power Control

SUPPLY CONDITION	READ/WRITE ACCESS	POWERED BY
$V_{CC} < V_{PF}$, $V_{CC} < V_{BACKPUP}$	No	V_{BACKUP}
$V_{CC} < V_{PF}$, $V_{CC} > V_{BACKUP}$	No	V_{CC}
$V_{CC} > V_{PF}$, $V_{CC} < V_{BACKUP}$	Yes	V_{CC}
$V_{CC} > V_{PF}$, $V_{CC} > V_{BACKUP}$	Yes	V_{CC}

Oscillator Circuit

The DS1388 uses an external 32.768kHz crystal. The oscillator circuit does not require any external resistors or capacitors to operate. Table 2 specifies several crystal parameters for the external crystal. Using a crystal with the specified characteristics, the startup time is usually less than one second.

Table 2. Crystal Specifications*

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Nominal Frequency	f_O		32.768		kHz
Series Resistance	ESR			50	kΩ
Load Capacitance	C_L		6		pF

**The crystal, traces, and crystal input pins should be isolated from RF generating signals. Refer to Application Note 58: Crystal Considerations for Dallas Real-Time Clocks for additional specifications.*

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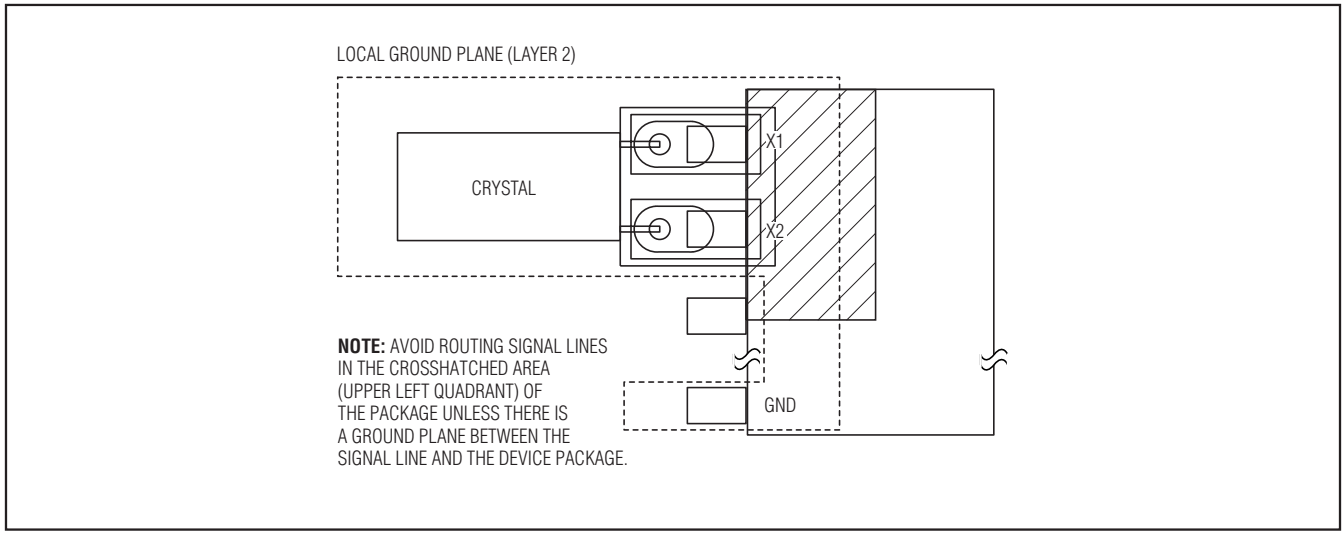

Figure 3. Layout Example

Clock Accuracy

The accuracy of the clock is dependent upon the accuracy of the crystal and the accuracy of the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. Additional error is added by crystal frequency drift caused by temperature shifts. External circuit noise coupled into the oscillator circuit can result in the clock running fast. Figure 3 shows a typical PC board layout for isolation of the crystal and oscillator from noise. Refer to Application Note 58: *Crystal Considerations with Dallas Real-Time Clock*s for detailed information.

Address Map

Figure 4 shows the address map for the DS1388. The memory map is divided into three blocks. The memory block accessed is determined by the value of the block address bits in the slave address byte. The timekeeping registers reside in block 0h. During a multibyte access of the timekeeping registers, when the internal address pointer reaches 0Ch, it wraps around to location 00h. On an I²C START or address pointer incrementing to location 00h, the current time is transferred to a second set of registers. The time information is read from these secondary registers, while the clock may continue to run. This eliminates the need to reread the registers in case the main registers update during a read. The EEPROM is divided into two 256-byte blocks located in blocks 1h and 2h. During a multibyte read of the EEPROM registers, when the internal address pointer reaches FFh, it wraps around to location 00h of the block of EEPROM specified in the block address. During a multibyte write of the EEPROM registers, when the internal address pointer reaches the end of the current 8-byte EEPROM page, it wraps around to the beginning of the EEPROM page. See the *Write Operation* section for details.

To avoid rollover issues when writing to the time and date registers, all registers should be written before the hundredths-of-seconds register reaches 99 (BCD).

Hundredths-of-Seconds Generator

The hundredths-of-seconds generator circuit shown in the *Block Diagram* is a state machine that divides the incoming frequency (4096Hz) by 41 for 24 cycles and 40 for 1 cycle. This produces a 100Hz output that is slightly off during the short term, and is exactly correct every 250ms. The divide ratio is given by:

$$\text{Ratio} = [41 \times 24 + 40 \times 1] / 25 = 40.96$$

Thus, the long-term average frequency output is exactly 100Hz.

ADDRESS		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	FUNCTION	RANGE
BLK	WORD										
0H	00H	Tenth Seconds				Hundredths of Seconds				Hundredths of Seconds	00–99
0H	01H	0	10 Seconds			Seconds				Seconds	00–59
0H	02H	0	10 Minutes			Minutes				Minutes	00–59
0H	03H	0	12/$\overline{24}$	$\overline{AM}$/PM	10 Hour	Hours				Hours	1–12+ $\overline{AM}$/PM 00–23
				10 Hour							
0H	04H	0	0	0	0	X	Day			Day	01–07
0H	05H	0	0	10 Date		Date				Date	00–31
0H	06H	0	0	X	10 Month	Month				Month	01–12
0H	07H	10 Year				Year				Year	00–99
0H	08H	Watchdog Tenths of Seconds				Watchdog Hundredths of Seconds				Watchdog Hundredth Seconds	00–99
0H	09H	Watchdog Tenths of Seconds				Watchdog Seconds				Watchdog Seconds	00–99
0H	0AH	TCS3	TCS2	TCS1	TCS0	DS1	DS0	ROUT1	ROUT0	Trickle Charger	—
0H	0BH	OSF	WF	0	0	0	0	0	0	Flag	—
0H	0CH	$\overline{EOSC}$	0	0	0	0	0	WDE	WD/$\overline{RST}$	Control	—
1H	00–FFH	256 x 8 EEPROM								EEPROM	00–FFh
2H	00–FFH	256 x 8 EEPROM								EEPROM	00–FFh

Figure 4. Address Map

Note: *Unless otherwise specified, the state of the registers is not defined when power (V_{CC} and V_{BACKUP}) is first applied.*

X = General-purpose read/write bit.

0 = Always reads as a zero.

Clock and Calendar

The time and calendar information is obtained by reading the appropriate register bytes. Figure 4 illustrates the RTC registers. The time and calendar are set or initialized by writing the appropriate register bytes. The contents of the time and calendar registers are in the binary-coded decimal (BCD) format. The end of the month date is automatically adjusted for months with fewer than 31 days, including corrections for leap years through 2099. The day-of-week register increments at midnight. Values that correspond to the day-of-week are user-defined but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday, and so on). Illogical time and date entries result in undefined operation. The DS1388 can be run in either 12-hour or 24-hour mode. Bit 6 of the hours register is defined as the 12- or 24-hour mode-select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the $\overline{AM}$/PM bit with logic-high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20–23 hours). Changing the 12/$\overline{24}$ bit requires that the hours data be re-entered in the proper format.

I²C RTC/Supervisor with Trickle Charger and 512 Bytes EEPROM

Watchdog Alarm Counter

The contents of the watchdog alarm counter, which is a separate two-byte BCD down counter, are accessed in the address range 08h–09h in block 0h. It is programmable in 10ms intervals from 0.01 to 99.99 seconds. When this counter is written, both the counter and a seed register are loaded with the desired value. When the counter is to be reloaded, it uses the value in the seed register. When the counter is read, the current counter value is latched into a register, which is output on the serial data line and the watchdog counter reloads the seed value.

If the counter is not needed, it can be disabled and used as a 16-bit cache of battery-backed RAM by setting the WDE bit in the control register to logic 0. If all 16 bits of the watchdog alarm counter are written to a zero when WDE = 1, the counter is disabled and the WF bit is not set.

When the WDE bit in the control register is set to a logic 1 and a non-zero value is written into the watchdog registers, the watchdog alarm counter decrements every 1/100 second, until it reaches zero. At this point, the WF bit in the flag register is set. If WD/$\overline{RST}$ = 1, the $\overline{RST}$ pin is pulsed low for t_{RST} and access to the DS1388 is inhibited. At the end of t_{RST}, the $\overline{RST}$ pin becomes high impedance, and read/write access to the DS1388 is enabled. The WF flag remains set until cleared by writing WF to logic 0. The watchdog alarm counter can be reloaded and restarted before the counter reaches zero by reading or writing any of the watchdog alarm counter registers.

The WDE bit must be set to zero before writing the watchdog registers. After writing the watchdog registers, WDE must be set to one to enable the watchdog.

Power-Up/Down, Reset, and Pushbutton Reset Functions

A precision temperature-compensated reference and comparator circuit monitors the status of V_{CC}. When an out-of-tolerance condition occurs, an internal power-fail signal is generated that blocks read/write access to the device and forces the $\overline{RST}$ pin low. When V_{CC} returns to an in-tolerance condition, the internal power-fail signal is held active for t_{RST} to allow the power supply to stabilize, and the $\overline{RST}$ pin is held low. If the $\overline{EOSC}$ bit is set to a logic 1 (to disable the oscillator in battery-backup mode), the internal power-fail signal and the $\overline{RST}$ pin are kept active for t_{RST} plus the oscillator startup time. Access is inhibited whenever $\overline{RST}$ is low.

The DS1388 provides for a pushbutton switch to be connected to the $\overline{RST}$ output pin. When the DS1388 is not in a reset cycle, it continuously monitors the $\overline{RST}$ signal for a low-going edge. If an edge is detected, the part debounces the switch by pulling the $\overline{RST}$ pin low and inhibits read/write access. After the internal timer has expired, the part continues to monitor the $\overline{RST}$ line. If the line is still low, it continues to monitor the line looking for a rising edge. Upon detecting release, the part forces the $\overline{RST}$ pin low and holds it low for t_{RST}.

Special-Purpose Registers

The DS1388 has three additional registers (control, flag, and trickle charger) that control the real-time clock, watchdog, and trickle charger.

Flag Register (00Bh)

Bit 7: Oscillator Stop Flag (OSF). A logic 1 in this bit indicates that the oscillator has stopped or was stopped for some period of time and may be used to judge the validity of the clock and calendar data. This bit is edge triggered and is set to logic 1 when the internal circuitry senses the oscillator has transitioned from a normal run state to a STOP condition. The following are examples of conditions that can cause the OSF bit to be set:

1) The first time power is applied.
2) The voltage present on both V_{CC} and V_{BACKUP} are insufficient to support oscillation.
3) The $\overline{EOSC}$ bit is turned off.
4) External influences on the crystal (i.e., noise, leakage, etc.).

This bit remains at logic 1 until written to logic 0. This bit can only be written to logic 0. Attempting to write OSF to logic 1 leaves the value unchanged.

Bit 6: Watchdog Alarm Flag (WF). A logic 1 in this bit indicates that the watchdog counter reached zero. If WDE and WD/$\overline{RST}$ are set to 1, the $\overline{RST}$ pin pulses low for t_{RST} when the watchdog counter reaches zero and sets WF = 1. At the completion of the pulse, the WF bit remains set to logic 1. Writing this bit to logic 0 clears the WF flag. This bit can only be written to logic 0. Attempting to write logic 1 leaves the value unchanged.

Bits 5 to 0: These bits read as zero and cannot be modified.

Flag Register (00Bh)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
OSF	WF	0	0	0	0	0	0

Control Register (00Ch)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$\overline{EOSC}$	0	0	0	0	0	WDE	WD/$\overline{RST}$

Control Register (00Ch)

Bit 7: Enable Oscillator ($\overline{EOSC}$). When set to logic 0, the oscillator is started. When set to logic 1, the oscillator is stopped when the DS1388 switches to battery power. This setting can be used to conserve battery power when timekeeping operation is not required. This bit is cleared (logic 0) when power is first applied. When the DS1388 is powered by V_{CC}, the oscillator is always on regardless of the status of the $\overline{EOSC}$ bit. The clock can be halted whenever the timekeeping functions are not required, which minimizes V_{BAT} current ($I_{BACKUPDR}$).

Bits 6 to 2: These bits read as zero and cannot be modified.

Bit 1: Watchdog Enable (WDE). When set to logic one, the watchdog counter is enabled. When set to logic 0, the watchdog counter is disabled, and the two registers can be used as NV RAM. This bit is cleared (logic 0) when power is first applied.

Bit 0: Watchdog Reset (WD/$\overline{RST}$). This bit enables the watchdog alarm output to drive the $\overline{RST}$ pin. When the WD/$\overline{RST}$ bit is set to logic 1, $\overline{RST}$ pulses low for t_{RST} if WDE = 1 and the watchdog counter reaches zero. When the WD/$\overline{RST}$ bit is set to logic 0, the $\overline{RST}$ pin is not driven by the watchdog alarm; only the watchdog flag bit (WF) in the flag register is set to logic 1. This bit is logic 0 when power is first applied.

Trickle-Charge Register (00Ah)

The simplified schematic of Figure 5 shows the basic components of the trickle charger. The trickle-charge select (TCS) bits (bits 4–7) control the selection of the trickle charger. To prevent accidental enabling, only a pattern on 1010 enables the trickle charger. All other patterns disable it. The trickle charger is disabled when power is first applied. The diode-select (DS) bits (bits 2 and 3) select whether or not a diode is connected between V_{CC} and V_{BACKUP}. If DS is 01, no diode is selected, yet if DS is 10, a diode is selected. The ROUT bits (bits 0 and 1) select the value of the resistor connected between V_{CC} and V_{BACKUP}. Table 3 shows the resistor selected by the resistor select (ROUT) bits and the diode selected by the diode-select (DS) bits.

Warning: The ROUT value of 250Ω must not be selected whenever V_{CC} is greater than 3.63V.

The user determines the diode and resistor selection according to the maximum current desired for battery or super cap charging. The maximum charging current can be calculated as illustrated in the following example. Assume that a system power supply of 3.3V is applied to V_{CC} and a super cap is connected to V_{BACKUP}. Also, assume that the trickle charger has been enabled with a diode and resistor R2 between V_{CC} and V_{BACKUP}. The maximum current I_{MAX} would be calculated as follows:

$$I_{MAX} = (3.3V - \text{diode drop}) / R2 \approx (3.3V - 0.7V) / 2k\Omega \approx 1.3mA$$

As the super cap charges, the voltage drop between V_{CC} and V_{BACKUP} decreases and therefore the charge current decreases.

Table 3. Trickle-Charge Register

TCS3	TCS2	TCS1	TCS0	DS1	DS0	ROUT1	ROUT0	FUNCTION
X	X	X	X	0	0	X	X	Disabled
X	X	X	X	1	1	X	X	Disabled
X	X	X	X	X	X	0	0	Disabled
1	0	1	0	0	1	0	1	No diode, 250Ω resistor
1	0	1	0	1	0	0	1	One diode, 250Ω resistor
1	0	1	0	0	1	1	0	No diode, 2kΩ resistor
1	0	1	0	1	0	1	0	One diode, 2kΩ resistor
1	0	1	0	0	1	1	1	No diode, 4kΩ resistor
1	0	1	0	1	0	1	1	One diode, 4kΩ resistor
0	0	0	0	0	0	0	0	Initial default value—disabled

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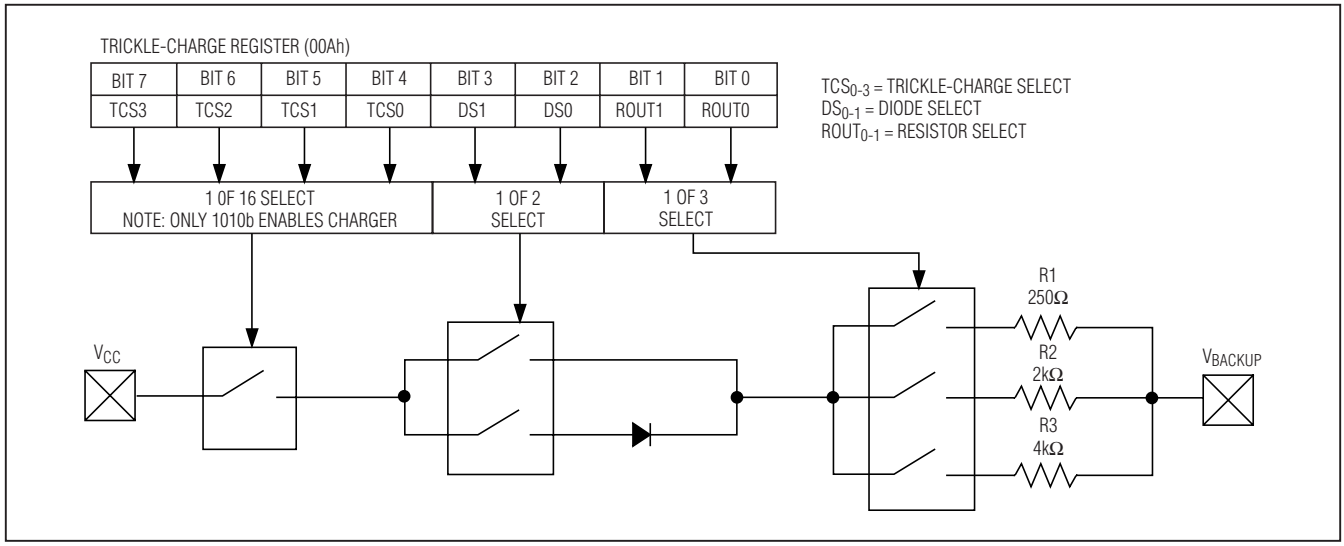

Figure 5. Programmable Trickle Charger

EEPROM

The DS1388 provides 512 bytes of EEPROM organized into two blocks of 256 bytes. Each 256-byte block is divided into 32 pages consisting of 8 bytes per page. The EEPROM can be written one page at a time. Page write operations are limited to writing bytes within a single physical page, regardless of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page size (8 bytes) and end at addresses that are integer multiples of [page size -1]. For example, page 0 contains word addresses 00h to 07h. Similarly, page 1 contains word addresses 08h to 0Fh. If a page write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page as might be expected. Therefore, it is necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

I²C Serial Data Bus

The DS1388 supports a bidirectional I²C bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data is defined as a receiver. The device that controls the message is called a master. The devices that are controlled by the master are slaves. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The DS1388 operates as a slave on the I²C bus. Connections to the bus are made through the open-drain I/O lines SDA and SCL. Within the bus specifications, a standard mode (100kHz maximum clock rate) and a fast mode (400kHz maximum clock rate) are defined. The DS1388 works in both modes.

The following bus protocol has been defined (Figure 6):

- Data transfer can be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain high.

Start data transfer: A change in the state of the data line from high to low, while the clock line is high, defines a START condition.

Stop data transfer: A change in the state of the data line from low to high, while the clock line is high, defines a STOP condition.

Data valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the high period of the clock signal. The data on the line must be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between the START and the STOP conditions is not limited, and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge (ACK) after the reception of each byte. The master device must generate an extra clock pulse, which is associated with this acknowledge bit. The DS1388 does not generate any acknowledge bits if access to the EEPROM is attempted during an internal programming cycle.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by generating a not-acknowledge (NACK) bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line high to enable the master to generate the STOP condition.

Figures 7 and 8 detail how data transfer is accomplished on the I²C bus. Depending upon the state of the R/$\overline{W}$ bit, two types of data transfer are possible:

Data transfer from a master transmitter to a slave receiver. The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. Data are transferred with the most significant bit (MSB) first.

Data transfer from a slave transmitter to a master receiver. The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit. Next follows a number of data bytes transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a NACK is returned.

The master device generates all the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus is not released. Data are transferred with the most significant bit (MSB) first.

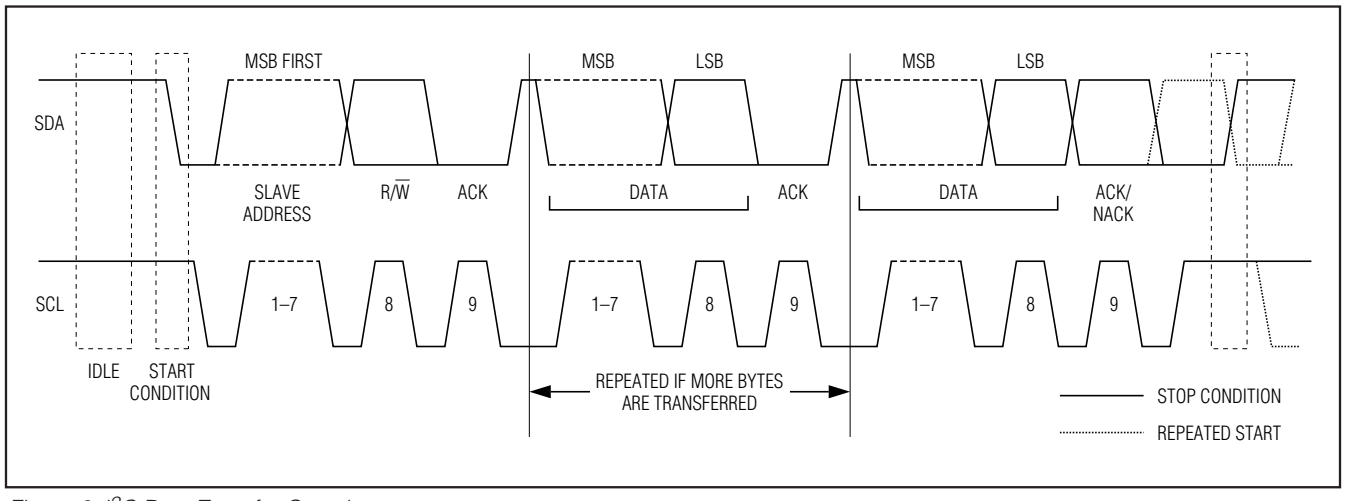

Figure 6. I²C Data Transfer Overview

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Device Addressing

The slave address byte is the first byte received following the START condition from the master device. The slave address byte consists of a 4-bit control code. For the DS1388, this is set as 1101 binary for read and write operations. The next three bits of the slave address byte are the block select bits (B2, B1, B0). B2 is always logic 0 for the DS1388. These bits are used by the master device to select which of the three blocks in the memory map are to be accessed. These bits are the three most significant bits of the word address. The last bit of the slave address byte defines the operation to be performed. When set to 1, a read operation is selected; when set to 0, a write operation is selected.

Write Operation

Slave Receiver Mode (Write Mode)

Following the START condition from the master, the device code (4 bits); the block address (3 bits); and the R/$\overline{W}$ bit, which is logic-low, is placed onto the bus by the master transmitter. This indicates to the DS1388 that a byte with a word address follows after the DS1388 has generated an acknowledge bit during the ninth clock cycle. The next byte transmitted by the master is the word address and will set the internal address pointer of the DS1388, with the DS1388 acknowledging the transfer on the ninth clock cycle. The master device can then transmit zero or more bytes of data, with the DS1388 acknowledging the transfer on the ninth clock cycle. The master generates a STOP condition to terminate the data write.

Byte Write

The write-slave address byte and word address are transmitted to the DS1388 as described in the *Slave Receiver Mode* section. The master transmits one data byte, with the DS1388 acknowledging the transfer on the ninth clock cycle. The master then generates a STOP condition to terminate the data write. This initiates the internal write cycle, and, if the write was to the EEPROM, the DS1388 does not generate acknowledge signals during the internal EEPROM write cycle.

EEPROM Page Write

The write-slave address byte, word address, and the first data byte are transmitted to the DS1388 in the same way as in a byte write. But instead of generating a STOP condition, the master transmits up to 8 data bytes to the DS1388, which are temporarily stored in the on-chip page buffer and are written into the memory after the master has transmitted a STOP condition. Data bytes within the page that are not written remain unchanged. The internal address pointer automatically increments after each byte is written.

If the master should transmit more than 8 data bytes prior to generating the STOP condition, the address pointer rolls over and the previously received data is overwritten. As with the byte write operation, once the STOP condition is received an internal write cycle begins.

RTC Multibyte Write

Writing multiple bytes to the RTC works much the same way as the EEPROM page write, except that the entire contents of block 0h can be written at once. The 8-byte page size limitation does not apply to the block 0. If the master should transmit more bytes than exists in block 0 prior to generating the STOP condition, the internal address pointer rolls over and the previously received data is overwritten. As with the byte write operation, once the STOP condition is received an internal write cycle begins.

Slave Address Byte

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
1	1	0	1	B2	B1	B0	R/$\overline{W}$

OPERATION	CONTROL CODE	BLOCK SELECT	R/$\overline{W}$
Read Clock	1101	000	1
Write Clock	1101	000	0
Read Lower Block of EEPROM	1101	001	1
Write Lower Block of EEPROM	1101	001	0
Read Upper Block of EEPROM	1101	010	1
Write Upper Block of EEPROM	1101	010	0

Acknowledge Polling

Since the DS1388 does not acknowledge during an EEPROM write cycle, acknowledge polling can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the master issues the STOP condition for a write command, the DS1388 initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a START condition, followed by the slave address byte for a write command (R/$\overline{W}$ = 0) to the EEPROM. If the device is still busy with the write cycle, then a NACK is returned. If the cycle is complete, then the device returns the ACK and the master can then proceed with the next read or write command. The RTC registers in block 0 are accessible during an EEPROM write cycle.

Read Operation

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to 1. There are three basic types of read operations: current address read, random read, and sequential read.

Current Address Read

The DS1388 contains an address pointer that maintains the last address accessed, internally incremented by 1. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with the R/$\overline{W}$ bit set to 1, the DS1388 issues an acknowledge and transmits the 8-bit data byte. The master issues a NACK followed by a STOP condition, and the DS1388 discontinues transmission.

Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the DS1388 as part of a write operation. After the word address is sent, the master generates a START condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the slave address byte again but with the R/$\overline{W}$ bit set to 1. The DS1388 then issues an acknowledge and transmits the 8-bit data byte. The master issues a NACK followed by a STOP condition, and the DS1388 discontinues transmission.

Sequential Read

Sequential reads are initiated in the same way as a random read except that after the DS1388 transmits the first data byte, the master issues an acknowledge as opposed to a STOP condition in a random read. This directs the DS1388 to transmit the next sequentially addressed 8-bit byte. To provide sequential reads, the DS1388 contains an internal address pointer, which is incremented by one at the completion of each operation. This allows the entire memory contents of the block specified in the slave address to be serially read during one operation. The master terminates the read by generating a NACK followed by a STOP condition.

No page boundaries exist for read operations. When the address pointer reaches the end of an EEPROM block (FFh), the address pointer wraps to the beginning (00h) of the same block.

The DS1388 can operate in the two modes illustrated in Figures 7 and 8.

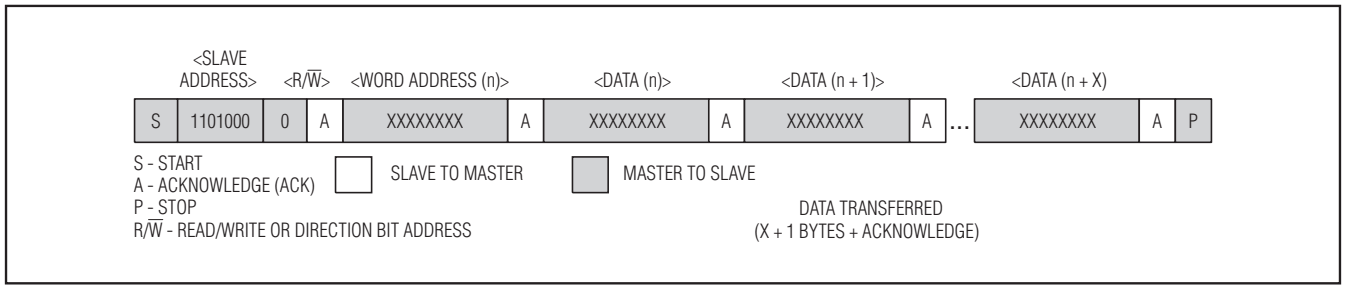

Figure 7. Data Write—Slave Receiver Mode

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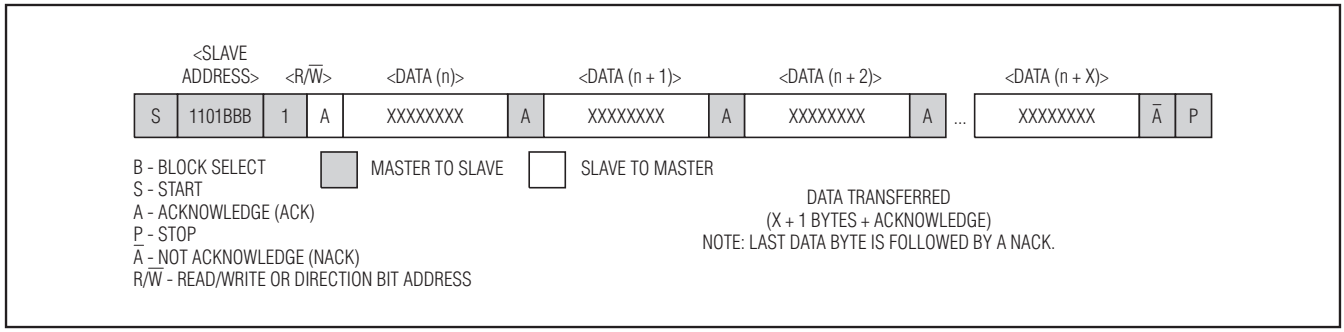

Figure 8. Data Read—Slave Transmitter Mode

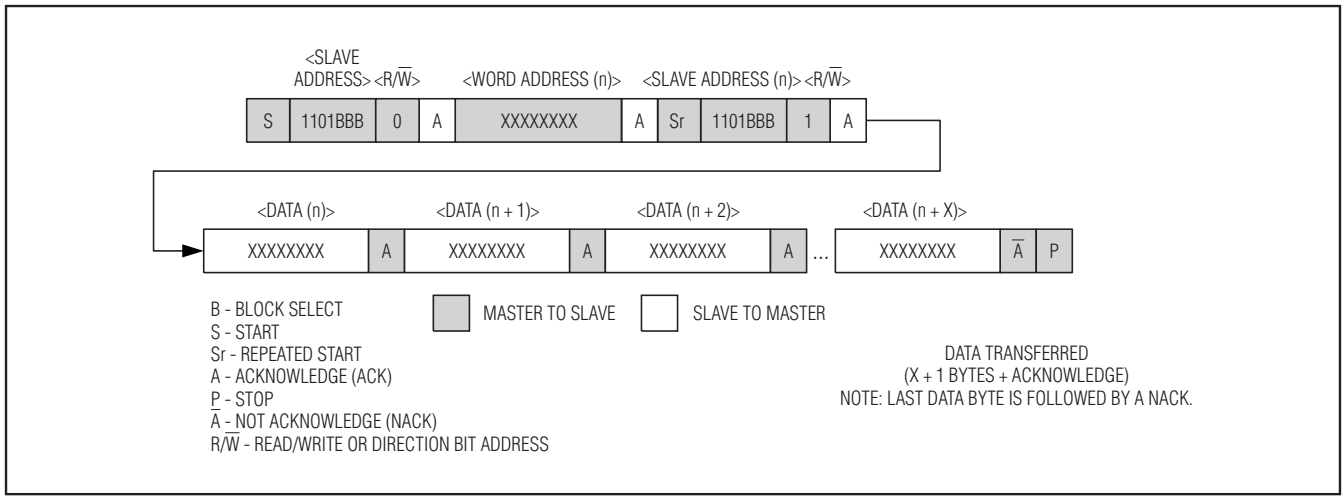

Figure 9. Data Write/Read (Write Pointer, Then Read)—Slave Receive and Transmit

Thermal Information

Theta-JA: +170°C/W

Theta-JC: +40°C/W

Chip Information

TRANSISTOR COUNT: 25,527

SUBSTRATE CONNECTED TO GROUND

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
8 SO	—	21-0041

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/05	Initial release.	—
1	9/08	Removed the leaded parts from the *Ordering Information*.	1
		Indicated the pullup voltage for SDA and SCL in the *Pin Description* table.	8
		Added the oscillator bias circuit to the *Block Diagram* and removed the original Figure 3.	8, 10
		Added time and date POR values in the *Power Control* section.	9
		Changed the last sentence of the *Watchdog Alarm Counter* section (first paragraph) to "When the counter is read, the current counter value is latched into a register, which is output on the serial data line and the watchdog counter reloads the seed value."	12
		Added "Access is inhibited whenever $\overline{RST}$ is low." To the end of the *Power-Up/Down, Reset, and Pushbutton Reset Functions* section (first paragraph).	12
		In the *Control Register (00Ch)* section, bit 7 description, added a statement that $\overline{EOSC}$ is used to reduce V_{BAT} current when timekeeping is not required.	13
		Replaced the I²C read and write figures.	17, 18