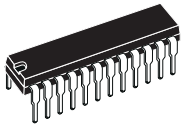
L6207

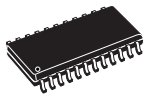
DMOS DUAL FULL BRIDGE DRIVER WITH PWM CURRENT CONTROLLER

- OPERATING SUPPLY VOLTAGE FROM 8 TO 52V
- 5.6A OUTPUT PEAK CURRENT (2.8A DC)
- $R_{DS(ON)}$ 0.3Ω TYP. VALUE @ T_j = 25 °C
- OPERATING FREQUENCY UP TO 100KHz
- NON DISSIPATIVE OVERCURRENT PROTECTION
- DUAL INDEPENDENT CONSTANT t_{OFF} PWM CURRENT CONTROLLERS
- SLOW DECAY SYNCHRONOUS RECTIFICATION
- CROSS CONDUCTION PROTECTION
- THERMAL SHUTDOWN
- UNDER VOLTAGE LOCKOUT
- INTEGRATED FAST FREE WHEELING DIODES



PowerDIP24 (20+2+2)

PowerSO36



SO24 (20+2+2)

ORDERING NUMBERS:
L6207N (PowerDIP24)
L6207PD (PowerSO36)
L6207D (SO24)

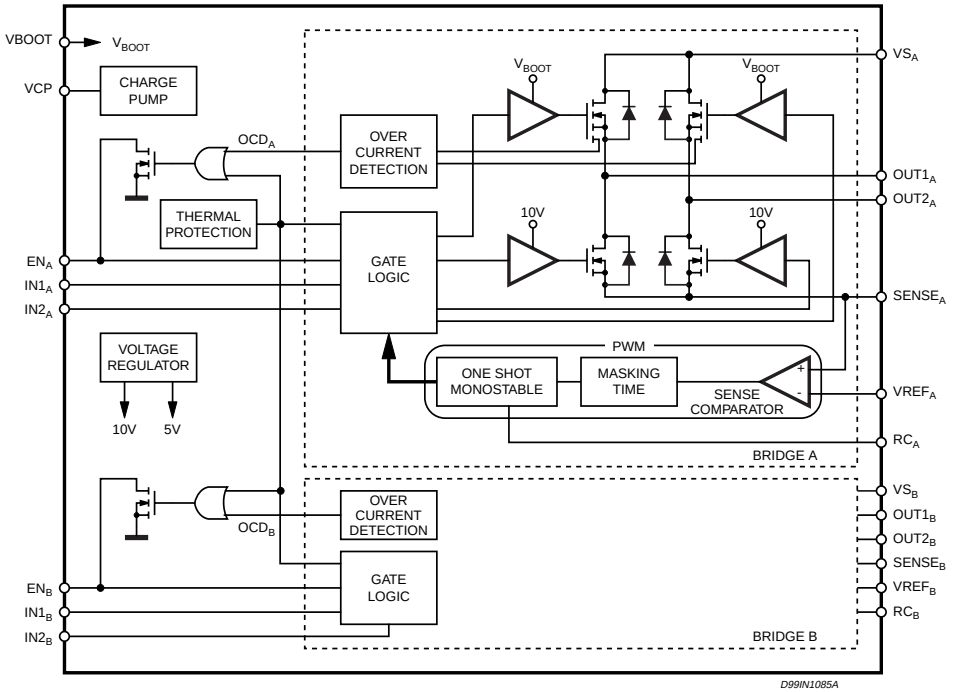
TYPICAL APPLICATIONS

- BIPOLAR STEPPER MOTOR
- DUAL DC MOTOR

DESCRIPTION

The L6207 is a DMOS Dual Full Bridge designed for motor control applications, realized in MultiPower-BCD technology, which combines isolated DMOS Power Transistors with CMOS and bipolar circuits on the same chip. The device also includes two independent constant off time PWM Current Controllers that performs the chopping regulation. Available in PowerDIP24 (20+2+2), PowerSO36 and SO24 (20+2+2) packages, the L6207 features a non-dissipative overcurrent protection on the high side Power MOSFETs and thermal shutdown.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test conditions	Value	Unit
V_S	Supply Voltage	$V_{SA} = V_{SB} = V_S$	60	V
V_{OD}	Differential Voltage between VS_A, $OUT1_A$, $OUT2_A$, $SENSE_A$ and VS_B, $OUT1_B$, $OUT2_B$, $SENSE_B$	$V_{SA} = V_{SB} = V_S = 60V$; $V_{SENSEA} = V_{SENSEB} = GND$	60	V
V_{BOOT}	Bootstrap Peak Voltage	$V_{SA} = V_{SB} = V_S$	$V_S + 10$	V
V_{IN},V_{EN}	Input and Enable Voltage Range		-0.3 to +7	V
V_{REFA}, V_{REFB}	Voltage Range at pins V_{REFA} and V_{REFB}		-0.3 to +7	V
V_{RCA}, V_{RCB}	Voltage Range at pins RC_A and RC_B		-0.3 to +7	V
V_{SENSEA}, V_{SENSEB}	Voltage Range at pins $SENSE_A$ and $SENSE_B$		-1 to +4	V
$I_{S(peak)}$	Pulsed Supply Current (for each V_S pin), internally limited by the overcurrent protection	$V_{SA} = V_{SB} = V_S$; $t_{PULSE} < 1ms$	7.1	A
I_S	RMS Supply Current (for each V_S pin)	$V_{SA} = V_{SB} = V_S$	2.8	A
T_{stg}, T_{OP}	Storage and Operating Temperature Range		-40 to 150	°C

RECOMMENDED OPERATING CONDITIONS

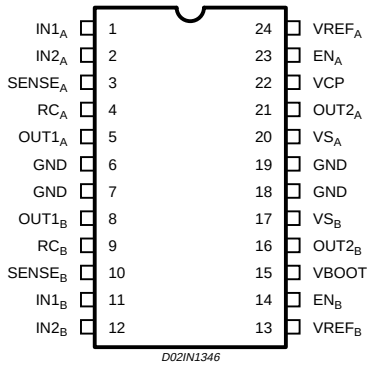
Symbol	Parameter	Test Conditions	MIN	MAX	Unit
V_S	Supply Voltage	$V_{SA} = V_{SB} = V_S$	8	52	V
V_{OD}	Differential Voltage Between VS_A, $OUT1_A$, $OUT2_A$, $SENSE_A$ and VS_B, $OUT1_B$, $OUT2_B$, $SENSE_B$	$V_{SA} = V_{SB} = V_S$; $V_{SENSEA} = V_{SENSEB}$		52	V
V_{REFA}, V_{REFB}	Voltage Range at pins V_{REFA} and V_{REFB}		-0.1	5	V
V_{SENSEA}, V_{SENSEB}	Voltage Range at pins $SENSE_A$ and $SENSE_B$	(pulsed $t_W < t_{rr}$) (DC)	-6 -1	6 1	V V
I_{OUT}	RMS Output Current			2.8	A
T_j	Operating Junction Temperature		-25	+125	°C
f_{sw}	Switching Frequency			100	KHz

THERMAL DATA

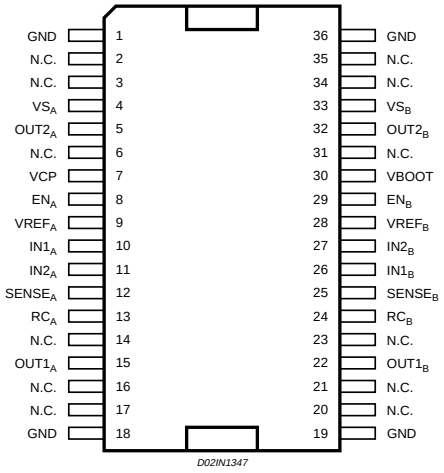
Symbol	Description	PowerDIP24	SO24	PowerSO36	Unit
$R_{th\text{-}j\text{-}pins}$	Maximum Thermal Resistance Junction-Pins	18	14	-	°C/W
$R_{th\text{-}j\text{-}case}$	Maximum Thermal Resistance Junction-Case	-	-	1	°C/W
$R_{th\text{-}j\text{-}amb1}$	Maximum Thermal Resistance Junction-Ambient [1]	43	51	-	°C/W
$R_{th\text{-}j\text{-}amb1}$	Maximum Thermal Resistance Junction-Ambient [2]	-	-	35	°C/W
$R_{th\text{-}j\text{-}amb1}$	Maximum Thermal Resistance Junction-Ambient [3]	-	-	15	°C/W
$R_{th\text{-}j\text{-}amb2}$	Maximum Thermal Resistance Junction-Ambient [4]	58	77	62	°C/W

(1) Mounted on a multi-layer FR4 PCB with a dissipating copper surface on the bottom side of 6cm^2 (with a thickness of 35µm).
(2) Mounted on a multi-layer FR4 PCB with a dissipating copper surface on the top side of 6cm^2 (with a thickness of 35µm).
(3) Mounted on a multi-layer FR4 PCB with a dissipating copper surface on the top side of 6cm^2 (with a thickness of 35µm), 16 via holes and a ground layer.
(4) Mounted on a multi-layer FR4 PCB without any heat sinking surface on the board.

PIN CONNECTIONS (Top View)



PowerDIP24/SO24



PowerSO36 (5)

(5) The slug is internally connected to pins 1,18,19 and 36 (GND pins).

PIN DESCRIPTION

PACKAGE		Name	Type	Function
SO24/ PowerDIP24	PowerSO36			
PIN #	PIN #			
1	10	$IN1_A$	Logic input	Bridge A Logic Input 1.
2	11	$IN2_A$	Logic input	Bridge A Logic Input 2.
3	12	$SENSE_A$	Power Supply	Bridge A Source Pin. This pin must be connected to Power Ground through a sensing power resistor.
4	13	RC_A	RC Pin	RC Network Pin. A parallel RC network connected between this pin and ground sets the Current Controller OFF-Time of the Bridge A.
5	15	$OUT1_A$	Power Output	Bridge A Output 1.
6, 7, 18, 19	1, 18, 19, 36	GND	GND	Signal Ground terminals. In Power DIP and SO packages, these pins are also used for heat dissipation toward the PCB.
8	22	$OUT1_B$	Power Output	Bridge B Output 1.
9	24	RC_B	RC Pin	RC Network Pin. A parallel RC network connected between this pin and ground sets the Current Controller OFF-Time of the Bridge B.
10	25	$SENSE_B$	Power Supply	Bridge B Source Pin. This pin must be connected to Power Ground through a sensing power resistor.
11	26	$IN1_B$	Logic Input	Bridge B Input 1
12	27	$IN2_B$	Logic Input	Bridge B Input 2
13	28	$VREF_B$	Analog Input	Bridge B Current Controller Reference Voltage. Do not leave this pin open or connect to GND.
14	29	EN_B	Logic Input (6)	Bridge B Enable. LOW logic level switches OFF all Power MOSFETs of Bridge B. This pin is also connected to the collector of the Overcurrent and Thermal Protection transistor to implement over current protection. If not used, it has to be connected to +5V through a resistor.
15	30	VBOOT	Supply Voltage	Bootstrap Voltage needed for driving the upper Power MOSFETs of both Bridge A and Bridge B.
16	32	$OUT2_B$	Power Output	Bridge B Output 2.
17	33	VS_B	Power Supply	Bridge B Power Supply Voltage. It must be connected to the supply voltage together with pin VS_A.
20	4	VS_A	Power Supply	Bridge A Power Supply Voltage. It must be connected to the supply voltage together with pin VS_B.
21	5	$OUT2_A$	Power Output	Bridge A Output 2.
22	7	VCP	Output	Charge Pump Oscillator Output.

PIN DESCRIPTION (continued)

23	8	EN_A	Logic Input (6)	Bridge A Enable. LOW logic level switches OFF all Power MOSFETs of Bridge A. This pin is also connected to the collector of the Overcurrent and Thermal Protection transistor to implement over current protection. If not used, it has to be connected to +5V through a resistor.
24	9	$VREF_A$	Analog Input	Bridge A Current Controller Reference Voltage. Do not leave this pin open or connect to GND.

(6) Also connected at the output drain of the Over current and Thermal protection MOSFET. Therefore, it has to be driven putting in series a resistor with a value in the range of 2.2KΩ - 180KΩ, recommended 100KΩ.

ELECTRICAL CHARACTERISTICS

(T_{amb} = 25 °C, V_S = 48V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{Sth(ON)}$	Turn-on Threshold		6.6	7	7.4	V
$V_{Sth(OFF)}$	Turn-off Threshold		5.6	6	6.4	V
I_S	Quiescent Supply Current	All Bridges OFF; T_j = -25°C to 125°C (7)		5	10	mA
$T_{j(OFF)}$	Thermal Shutdown Temperature			165		°C
Output DMOS Transistors						
$R_{DS(ON)}$	High-Side Switch ON Resistance	T_j = 25 °C		0.34	0.4	Ω
		T_j =125 °C (7)		0.53	0.59	Ω
	Low-Side Switch ON Resistance	T_j = 25 °C		0.28	0.34	Ω
		T_j =125 °C (7)		0.47	0.53	Ω
I_{DSS}	Leakage Current	EN = Low; OUT = V_S			2	mA
		EN = Low; OUT = GND	-0.15			mA
Source Drain Diodes						
V_{SD}	Forward ON Voltage	I_{SD} = 2.8A, EN = LOW		1.15	1.3	V
t_{rr}	Reverse Recovery Time	I_f = 2.8A		300		ns
t_{fr}	Forward Recovery Time			200		ns
Logic Input						
V_{IL}	Low level logic input voltage		-0.3		0.8	V
V_{IH}	High level logic input voltage		2		7	V
I_{IL}	Low Level Logic Input Current	GND Logic Input Voltage	-10			µA
I_{IH}	High Level Logic Input Current	7V Logic Input Voltage			10	µA
$V_{th(ON)}$	Turn-on Input Threshold			1.8	2.0	V
$V_{th(OFF)}$	Turn-off Input Threshold		0.8	1.3		V
$V_{th(HYS)}$	Input Threshold Hysteresis		0.25	0.5		V

ELECTRICAL CHARACTERISTICS (continued)
(T_{amb} = 25 °C, V_S = 48V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Switching Characteristics						
$t_{D(on)EN}$	Enable to out turn ON delay time (8)	I_{LOAD} =2.8A, Resistive Load	100	250	400	ns
$t_{D(on)IN}$	Input to out turn ON delay time	I_{LOAD} =2.8A, Resistive Load (dead time included)		1.6		µs
t_{RISE}	Output rise time(8)	I_{LOAD} =2.8A, Resistive Load	40		250	ns
$t_{D(off)EN}$	Enable to out turn OFF delay time (8)	I_{LOAD} =2.8A, Resistive Load	300	550	800	ns
$t_{D(off)IN}$	Input to out turn OFF delay time	I_{LOAD} =2.8A, Resistive Load		600		ns
t_{FALL}	Output Fall Time (8)	I_{LOAD} =2.8A, Resistive Load	40		250	ns
t_{dt}	Dead Time Protection		0.5	1		µs
f_{CP}	Charge pump frequency	-25°C<T_j <125°C		0.6	1	MHz
PWM Comparator and Monostable						
I_{RCA}, I_{RCB}	Source Current at pins RC_A and RC_B	V_{RCA} = V_{RCB} = 2.5V	3.5	5.5		mA
V_{offset}	Offset Voltage on Sense Comparator	V_{REFA}, V_{REFB} = 0.5V		±5		mV
t_{PROP}	Turn OFF Propagation Delay (9)			500		ns
t_{BLANK}	Internal Blanking Time on SENSE pins			1		µs
$t_{ON(MIN)}$	Minimum On Time			1.5	2	µs
t_{OFF}	PWM Recirculation Time	R_{OFF} = 20KΩ; C_{OFF} = 1nF		13		µs
		R_{OFF} = 100KΩ; C_{OFF} = 1nF		61		µs
I_{BIAS}	Input Bias Current at pins $VREF_A$ and $VREF_B$				10	µA
Over Current Protection						
I_{SOVER}	Input Supply Overcurrent Protection Threshold	T_j = -25°C to 125°C (7)	4	5.6	7.1	A
R_{OPDR}	Open Drain ON Resistance	I = 4mA		40	60	Ω
$t_{OCD(ON)}$	OCD Turn-on Delay Time (10)	I = 4mA; C_{EN} < 100pF		200		ns
$t_{OCD(OFF)}$	OCD Turn-off Delay Time (10)	I = 4mA; C_{EN} < 100pF		100		ns

(7) Tested at 25°C in a restricted range and guaranteed by characterization.
(8) See Fig. 1.
(9) Measured applying a voltage of 1V to pin SENSE and a voltage drop from 2V to 0V to pin VREF.
(10) See Fig. 2.

Figure 1. Switching Characteristic Definition

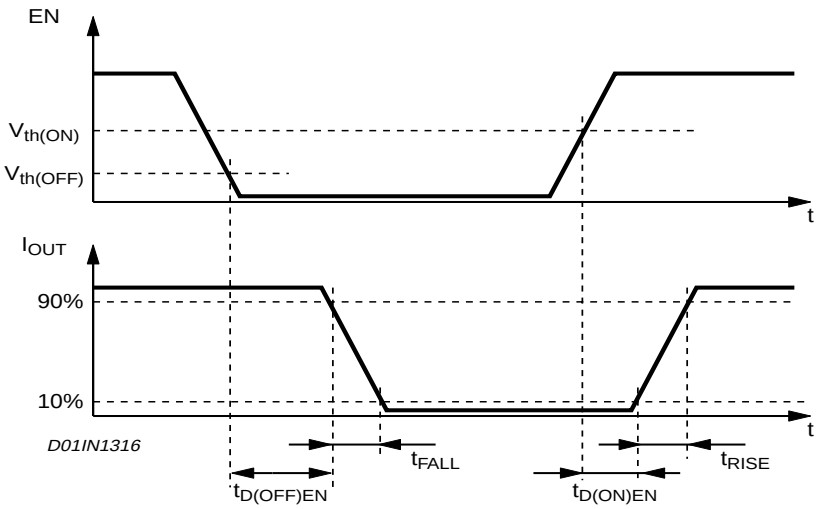
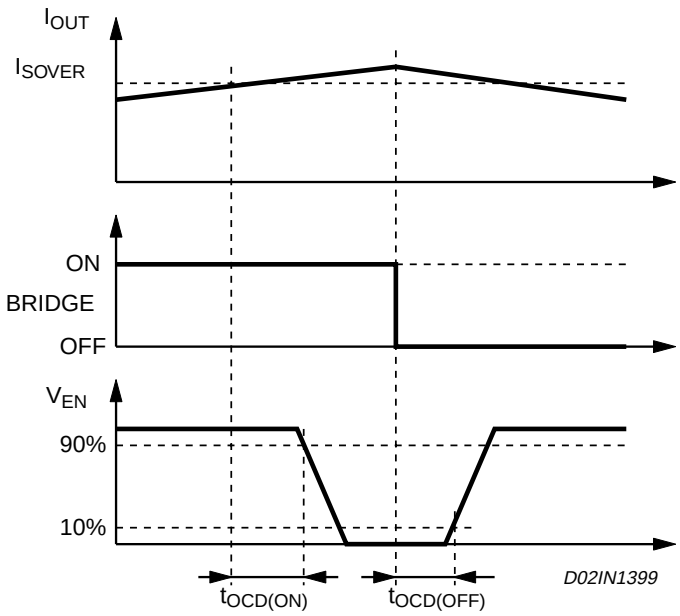


Figure 2. Overcurrent Detection Timing Definition



CIRCUIT DESCRIPTION

POWER STAGES and CHARGE PUMP

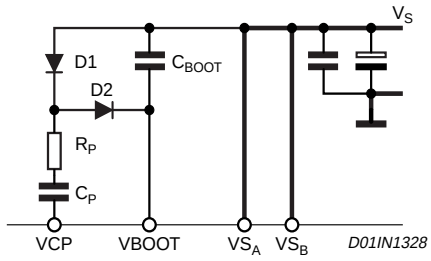
The L6207 integrates two independent Power MOS Full Bridges. Each Power MOS has an Rdson = 0.3ohm (typical value @ 25°C), with intrinsic fast freewheeling diode. Cross conduction protection is achieved using a dead time (td = 1µs typical) between the switch off and switch on of two Power MOS in one leg of a bridge.

Using N Channel Power MOS for the upper transistors in the bridge requires a gate drive voltage above the power supply voltage. The Bootstrapped (VBOOT) supply is obtained through an internal Oscillator and few external components to realize a charge pump circuit as shown in Figure 3. The oscillator output (VCP) is a square wave at 600kHz (typical) with 10V amplitude. Recommended values/part numbers for the charge pump circuit are shown in Table1.

Table 1. Charge Pump External Components Values

C_{BOOT}	220nF
C_P	10nF
R_P	100Ω
D1	1N4148
D2	1N4148

Figure 3. Charge Pump Circuit



LOGIC INPUTS

Pins $IN1_A$, $IN2_B$, $IN1_B$ and $IN2_B$ are TTL/CMOS and uC compatible logic inputs. The internal structure is shown in Fig. 4. Typical value for turn-on and turn-off thresholds are respectively Vthon = 1.8V and Vthoff = 1.3V.

Pins EN_A and EN_B have identical input structure with the exception that the drains of the Overcurrent and thermal protection MOSFETs (one for the Bridge A and one for the Bridge B) are also connected to these pins. Due to these connections some care needs to be taken in driving these pins. The EN_A and EN_B inputs may be driven in one of two configurations as shown in figures 5 or 6. If driven by an open drain (collector) structure, a pull-up resistor R_{EN} and a capacitor C_{EN} are connected as shown in Fig. 5. If the driver is a standard Push-Pull structure the resistor R_{EN} and the capacitor C_{EN} are connected as shown in Fig. 6. The resistor R_{EN} should be chosen in the range from 2.2kΩ to 180KΩ. Recommended values for R_{EN} and C_{EN} are respectively 100KΩ and 5.6nF. More information on selecting the values is found in the Overcurrent Protection section.

Figure 4. Logic Inputs Internal Structure

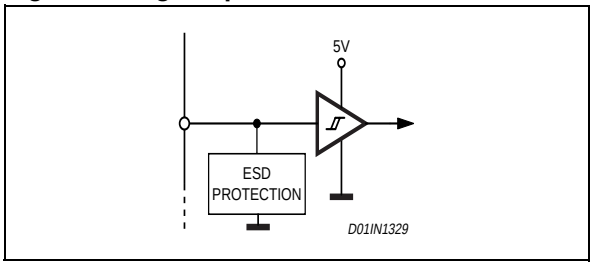


Figure 5. EN_A and EN_B Pins Open Collector Driving

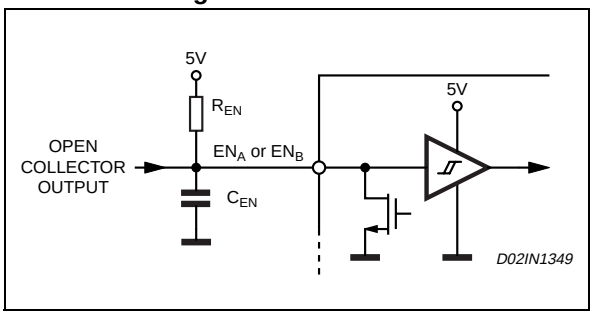
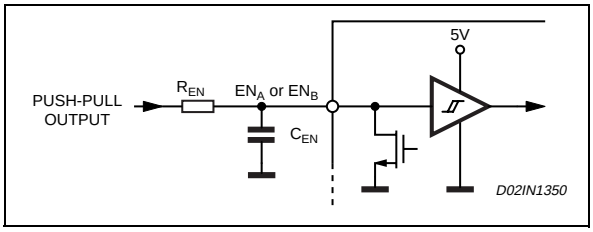


Figure 6. EN_A and EN_B Pins Push-Pull Driving



TRUTH TABLE

INPUTS			OUTPUTS		Description (*)
EN	IN1	IN2	OUT1	OUT2	
L	X	X	High Z	High Z	Disable
H	L	L	GND	GND	Brake Mode (Lower Path)
H	H	L	Vs	GND (Vs)	Forward
H	L	H	GND (Vs)	Vs	Reverse
H	H	H	Vs	Vs	Brake Mode (Upper Path)

X = Don't care
High Z = High Impedance Output
GND (Vs) = GND during Ton, Vs during Toff
(*) Valid only in case of load connected between OUT1 and OUT2

PWM CURRENT CONTROL

The L6207 includes a constant off time PWM current controller for each of the two bridges. The current control circuit senses the bridge current by sensing the voltage drop across an external sense resistor connected between the source of the two lower power MOS transistors and ground, as shown in Figure 7. As the current in the load builds up the voltage across the sense resistor increases proportionally. When the voltage drop across the sense resistor becomes greater than the voltage at the reference input ($VREF_A$ or $VREF_B$) the sense comparator triggers the monostable switching the low-side MOS off. The low-side MOS remain off for the time set by the monostable and the motor current recirculates in the upper path. When the monostable times out the bridge will again turn on. Since the internal dead time, used to prevent cross conduction in the bridge, delays the turn on of the power MOS, the effective off time is the sum of the monostable time plus the dead time.

Figure 7. PWM Current Controller Simplified Schematic

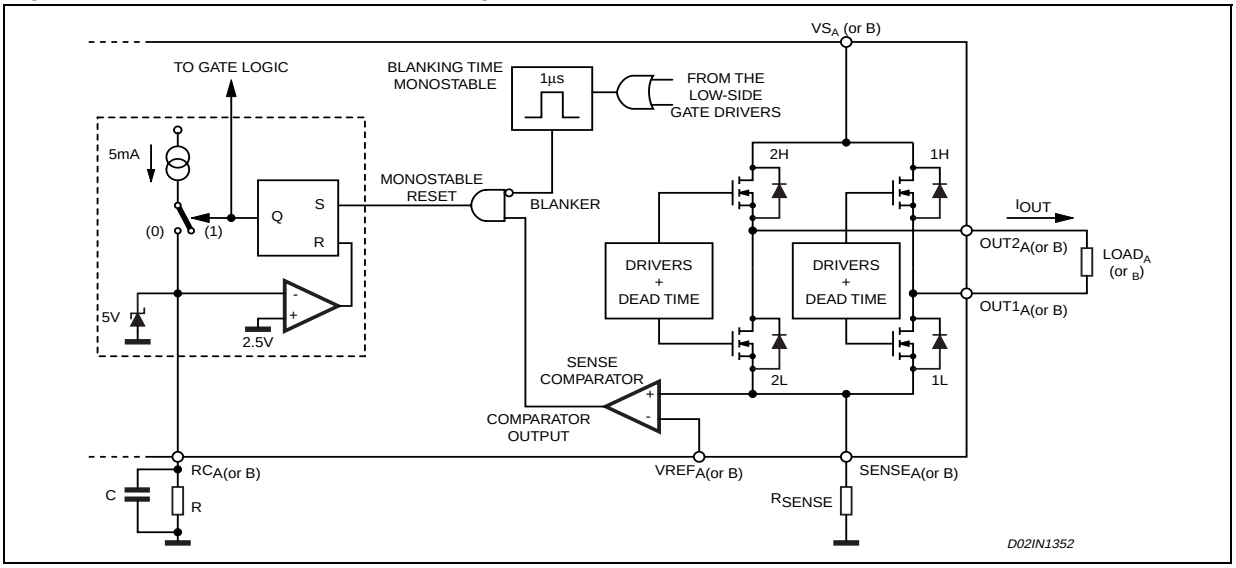


Figure 8 shows the typical operating waveforms of the output current, the voltage drop across the sensing resistor, the RC pin voltage and the status of the bridge. Immediately after the low-side Power MOS turns on, a high peak current flows through the sensing resistor due to the reverse recovery of the freewheeling diodes. The L6207 provides a 1µs Blanking Time t_{BLANK} that inhibits the comparator output so that this current spike cannot prematurely re-trigger the monostable.

Figure 8. Output Current Regulation Waveforms

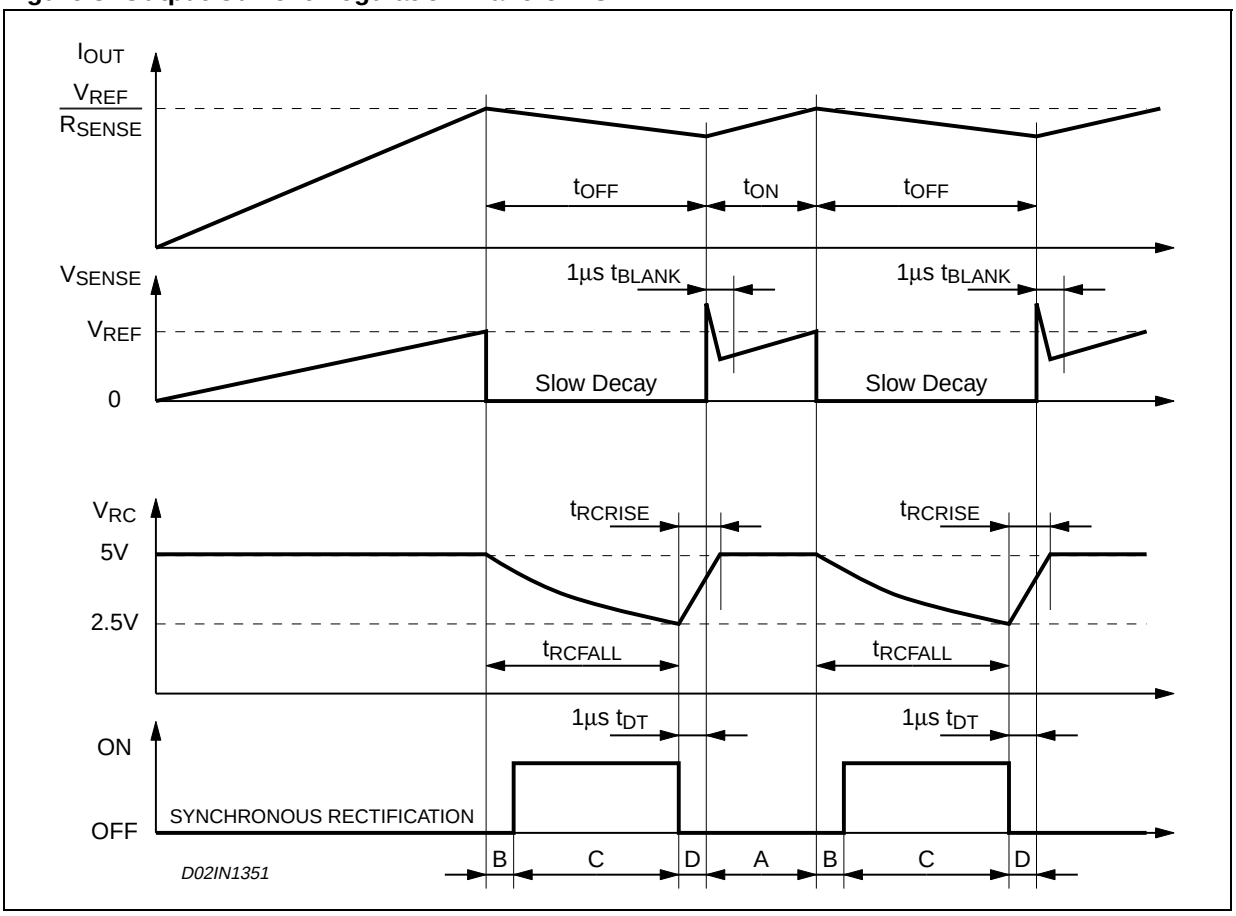


Figure 9 shows the magnitude of the Off Time t_{OFF} versus C_{OFF} and R_{OFF} values. It can be approximately calculated from the equations:

$t_{RCFALL} = 0.6 \cdot R_{OFF} \cdot C_{OFF}$

$t_{OFF} = t_{RCFALL} + t_{DT} = 0.6 \cdot R_{OFF} \cdot C_{OFF} + t_{DT}$

where R_{OFF} and C_{OFF} are the external component values and t_{DT} is the internally generated Dead Time with:

$20K\Omega \leq R_{OFF} \leq 100K\Omega$

$0.47nF \leq C_{OFF} \leq 100nF$

$t_{DT} = 1\mu s$ (typical value)

Therefore:

$t_{OFF(MIN)} = 6.6\mu s$

$t_{OFF(MAX)} = 6ms$

These values allow a sufficient range of t_{OFF} to implement the drive circuit for most motors.

The capacitor value chosen for C_{OFF} also affects the Rise Time t_{RCRISE} of the voltage at the pin RCOFF. The Rise Time t_{RCRISE} will only be an issue if the capacitor is not completely charged before the next time the monostable is triggered. Therefore, the on time t_{ON}, which depends by motors and supply parameters, has to

be bigger than t_{RCRISE} for allowing a good current regulation by the PWM stage. Furthermore, the on time t_{ON} can not be smaller than the minimum on time $t_{ON(MIN)}$.

$$\begin{cases} t_{ON} > t_{ON(MIN)} = 1.5\mu s \text{ (typ. value)} \\ t_{ON} > t_{RCRISE} - t_{DT} \end{cases}$$

$$t_{RCRISE} = 600 \cdot C_{OFF}$$

Figure 10 shows the lower limit for the on time t_{ON} for having a good PWM current regulation capacity. It has to be said that t_{ON} is always bigger than $t_{ON(MIN)}$ because the device imposes this condition, but it can be smaller than t_{RCRISE} - t_{DT}. In this last case the device continues to work but the off time t_{OFF} is not more constant.
So, small C_{OFF} value gives more flexibility for the applications (allows smaller on time and, therefore, higher switching frequency), but, the smaller is the value for C_{OFF}, the more influential will be the noises on the circuit performance.

Figure 9. t_{OFF} versus C_{OFF} and R_{OFF}

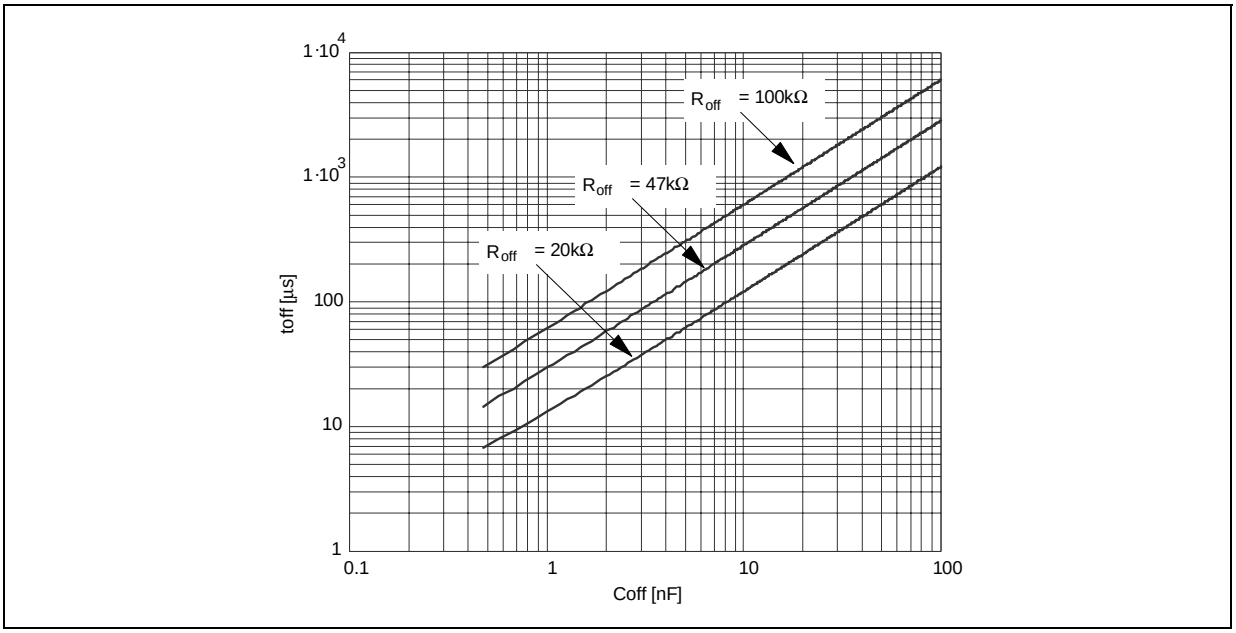
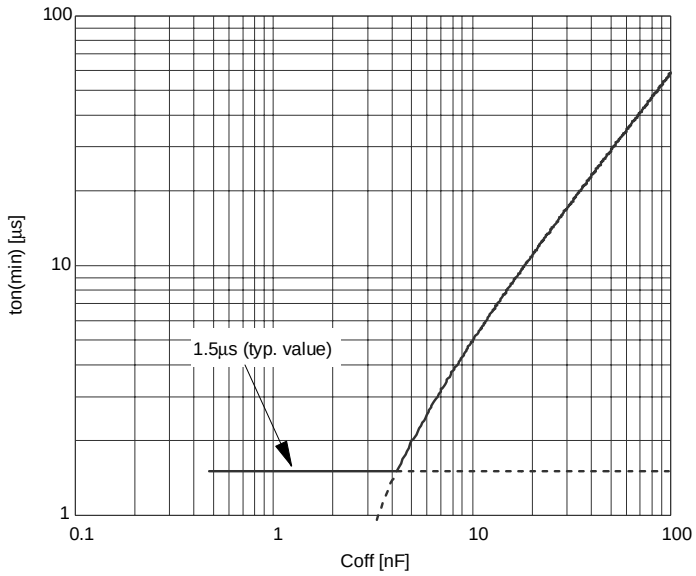


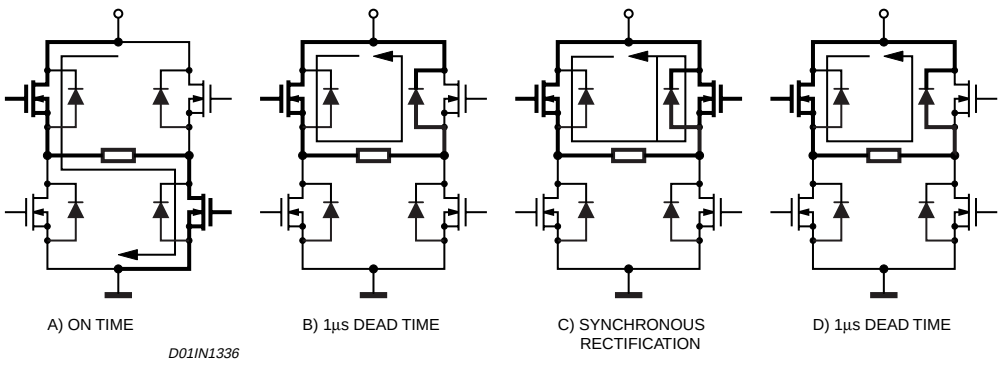
Figure 10. Area where t_{ON} can vary maintaining the PWM regulation.



SLOW DECAY MODE

Figure 11 shows the operation of the bridge in the Slow Decay mode. At the start of the off time, the lower power MOS is switched off and the current recirculates around the upper half of the bridge. Since the voltage across the coil is low, the current decays slowly. After the dead time the upper power MOS is operated in the synchronous rectification mode. When the monostable times out, the lower power MOS is turned on again after some delay set by the dead time to prevent cross conduction.

Figure 11. Slow Decay Mode Output Stage Configurations



NON-DISSIPATIVE OVERCURRENT PROTECTION

The L6207 integrates an Overcurrent Detection Circuit (OCD). This circuit provides protection against a short circuit to ground or between two phases of the bridge. With this internal over current detection, the external current sense resistor normally used and its associated power dissipation are eliminated. Figure 12 shows a simplified schematic of the overcurrent detection circuit.

To implement the over current detection, a sensing element that delivers a small but precise fraction of the output current is implemented with each high side power MOS. Since this current is a small fraction of the output current there is very little additional power dissipation. This current is compared with an internal reference current I_{REF}. When the output current in one bridge reaches the detection threshold (typically 5.6A) the relative OCD comparator signals a fault condition. When a fault condition is detected, the EN pin is pulled below the turn off threshold (1.3V typical) by an internal open drain MOS with a pull down capability of 4mA. By using an external R-C on the EN pin, the off time before recovering normal operation can be easily programmed by means of the accurate thresholds of the logic inputs.

Figure 12. Overcurrent Protection Simplified Schematic

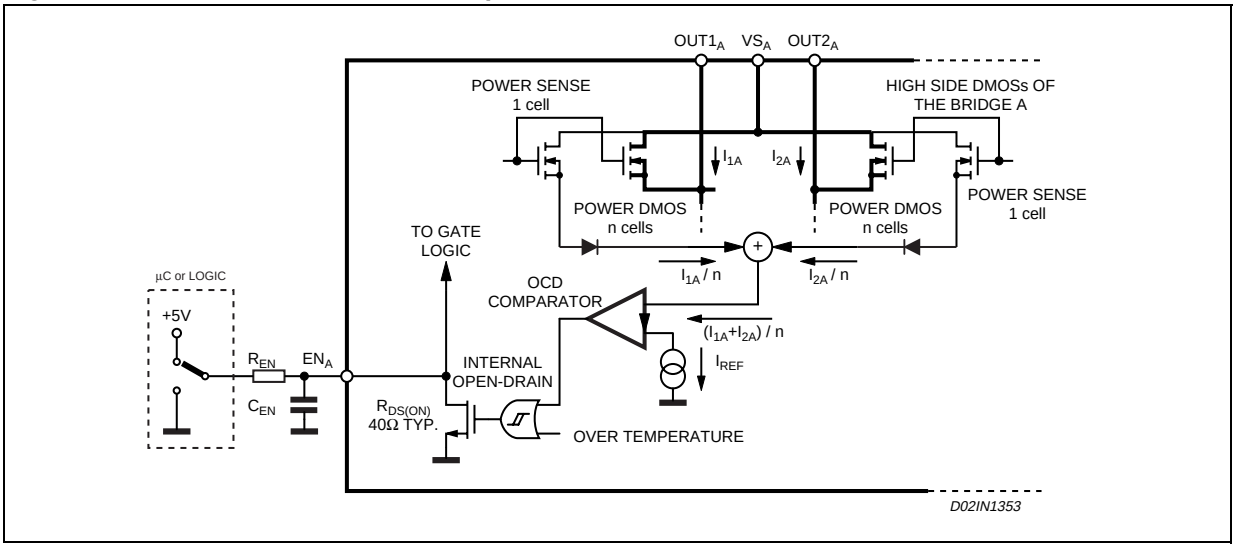


Figure 13 shows the Overcurrent Detection operation. The Disable Time $t_{DISABLE}$ before recovering normal operation can be easily programmed by means of the accurate thresholds of the logic inputs. It is affected whether by C_{EN} and R_{EN} values and its magnitude is reported in Figure 14. The Delay Time t_{DELAY} before turning off the bridge when an overcurrent has been detected depends only by C_{EN} value. Its magnitude is reported in Figure 15.

C_{EN} is also used for providing immunity to pin EN against fast transient noises. Therefore the value of C_{EN} should be chosen as big as possible according to the maximum tolerable Delay Time and the R_{EN} value should be chosen according to the desired Disable Time.

The resistor R_{EN} should be chosen in the range from 2.2KΩ to 180KΩ. Recommended values for R_{EN} and C_{EN} are respectively 100KΩ and 5.6nF that allow obtaining 200µs Disable Time.

Figure 13. Overcurrent Protection Waveforms

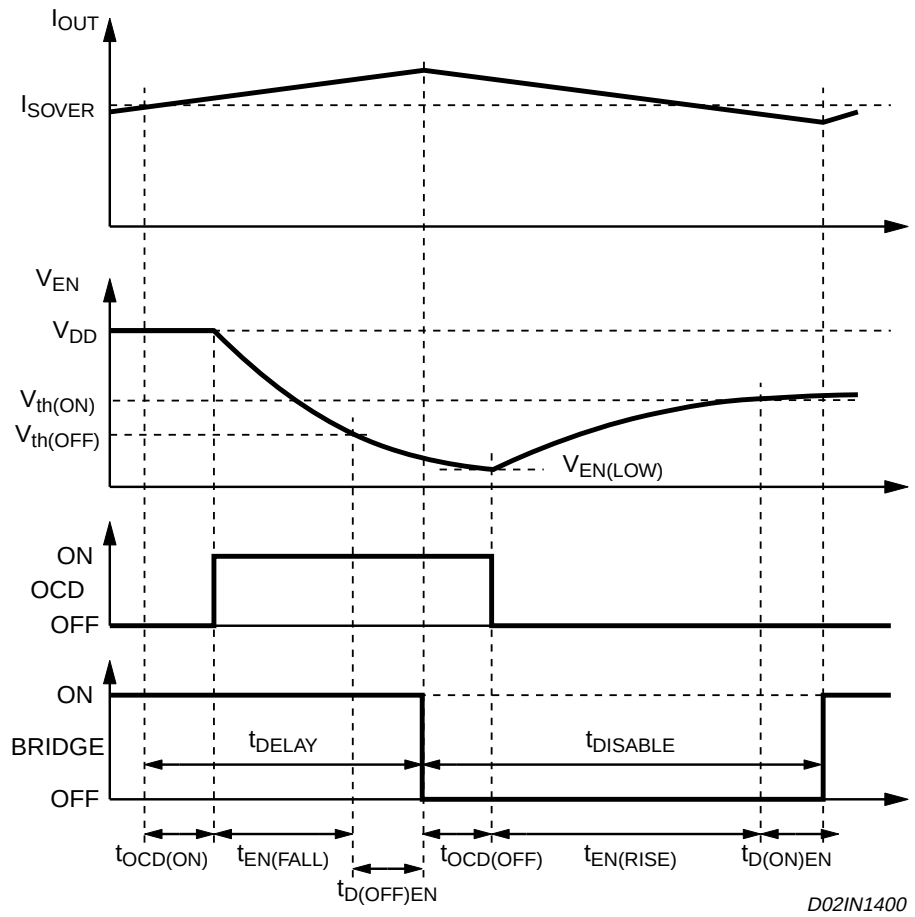


Figure 14. $t_{DISABLE}$ versus C_{EN} and R_{EN} (V_{DD} = 5V).

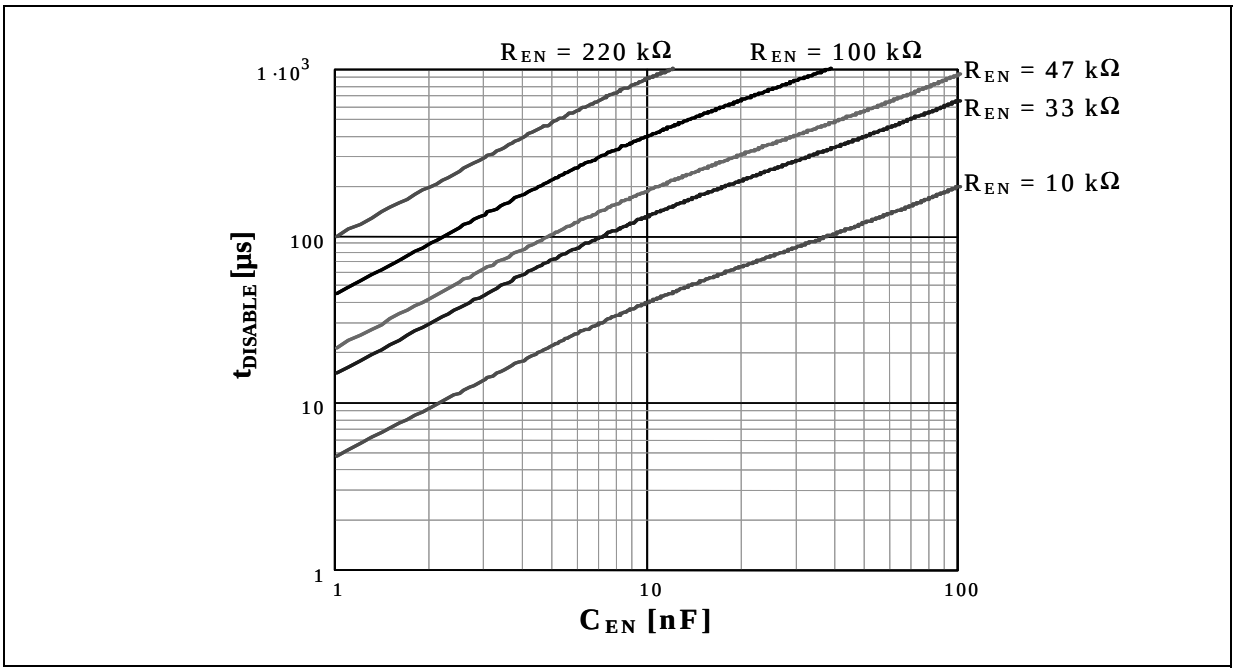
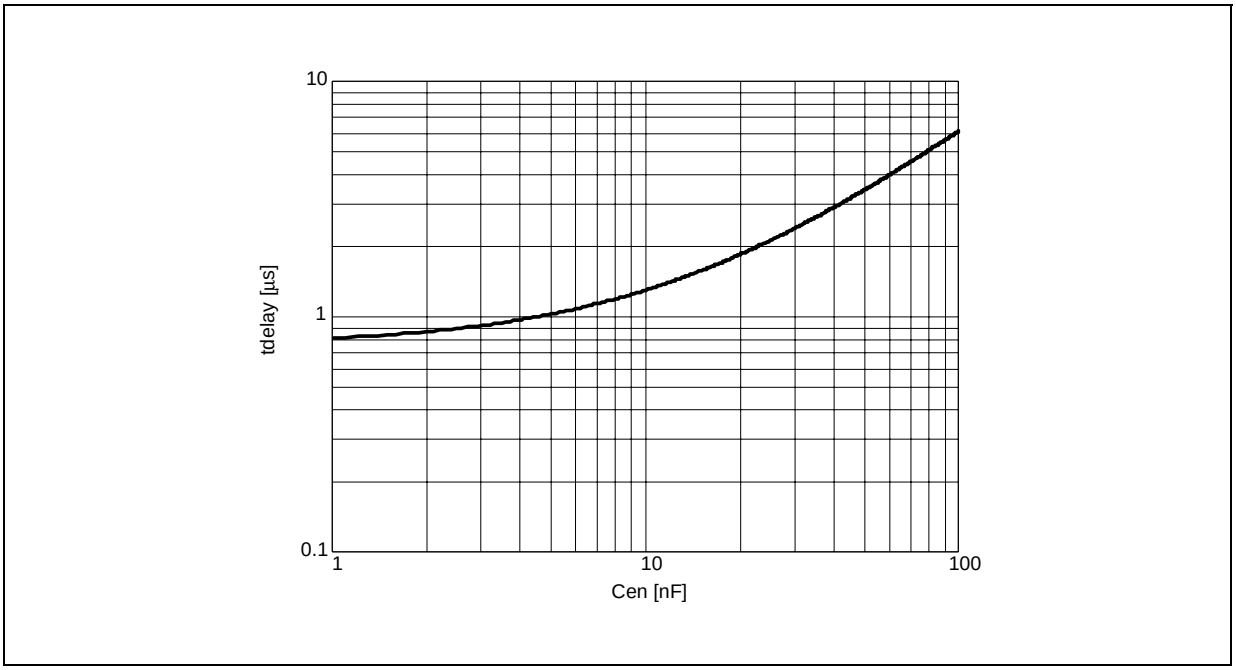


Figure 15. t_{DELAY} versus C_{EN} (V_{DD} = 5V).



THERMAL PROTECTION

In addition to the Ovecurrent Protection, the L6207 integrates a Thermal Protection for preventing the device destruction in case of junction over temperature. It works sensing the die temperature by means of a sensible element integrated in the die. The device switch-off when the junction temperature reaches 165°C (typ. value) with 15°C hysteresis (typ. value).

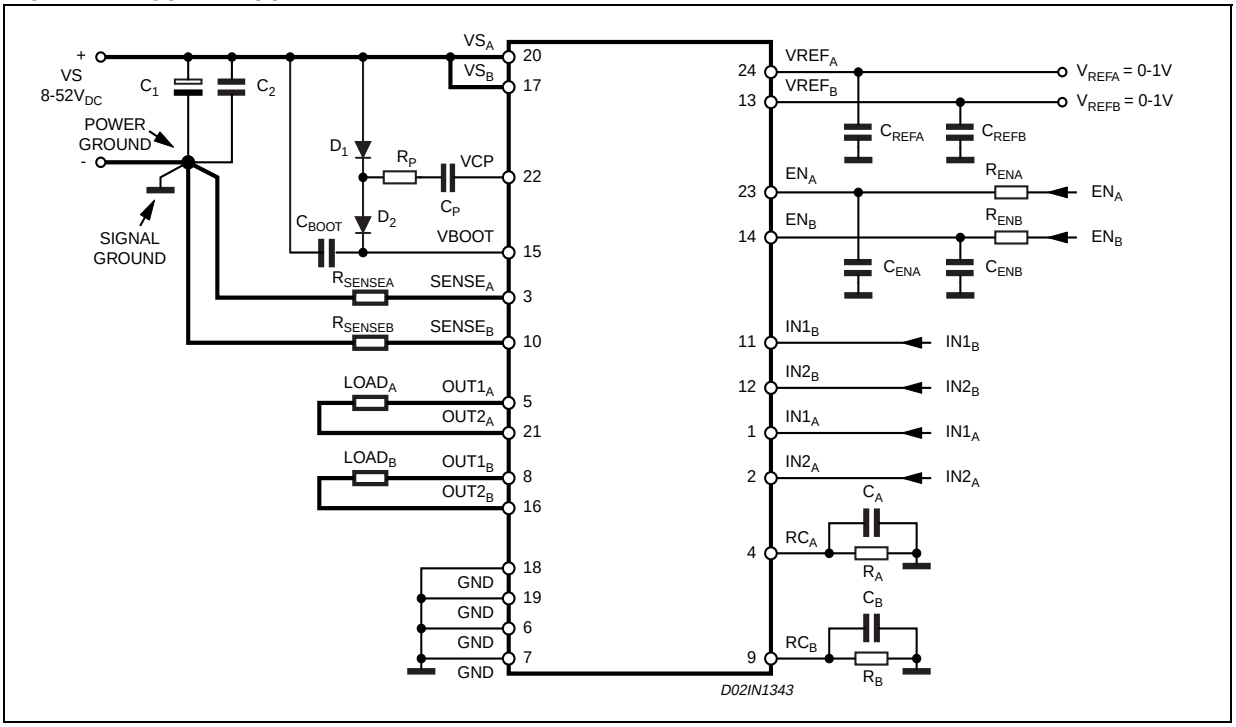
APPLICATION INFORMATION

A typical application using L6207 is shown in Fig. 16. Typical component values for the application are shown in Table 3. A high quality ceramic capacitor in the range of 100 to 200 nF should be placed between the power pins (VS_A and VS_B) and ground near the L6207 to improve the high frequency filtering on the power supply and reduce high frequency transients generated by the switching. The capacitors connected from the EN_A and EN_B inputs to ground set the shut down time for the BrgidgeA and BridgeB respectively when an over current is detected (see Overcurrent Protection). The two current sensing inputs ($SENSE_A$ and $SENSE_B$) should be connected to the sensing resistors with a trace length as short as possible in the layout. The sense resistors should be non-inductive resistors to minimize the di/dt transients across the resistor. To increase noise immunity, unused logic pins (except EN_A and EN_B) are best connected to 5V (High Logic Level) or GND (Low Logic Level) (see pin description). It is recommended to keep Power Ground and Signal Ground separated on PCB.

Table 2. Component Values for Typical Application

C_1	100uF	D_1	1N4148
C_2	100nF	D_2	1N4148
C_A	1nF	R_A	39KΩ
C_B	1nF	R_B	39KΩ
C_{BOOT}	220nF	R_{ENA}	100KΩ
C_P	10nF	R_{ENB}	100KΩ
C_{ENA}	5.6nF	R_P	100Ω
C_{ENB}	5.6nF	R_{SENSEA}	0.3Ω
C_{REFA}	68nF	R_{SENSEB}	0.3Ω
C_{REFB}	68nF		

Figure 16. Typical Application



OUTPUT CURRENT CAPABILITY AND IC POWER DISSIPATION

In Fig. 17 and Fig. 18 are shown the approximate relation between the output current and the IC power dissipation using PWM current control driving two loads, for two different driving types:

– One Full Bridge ON at a time (Fig.17) in which only one load at a time is energized.

– Two Full Bridges ON at the same time (Fig.18) in which two loads at the same time are energized.

For a given output current and driving type the power dissipated by the IC can be easily evaluated, in order to establish which package should be used and how large must be the on-board copper dissipating area to guarantee a safe operating junction temperature (125°C maximum).

Figure 17. IC Power Dissipation versus Output Current with One Full Bridge ON at a time.

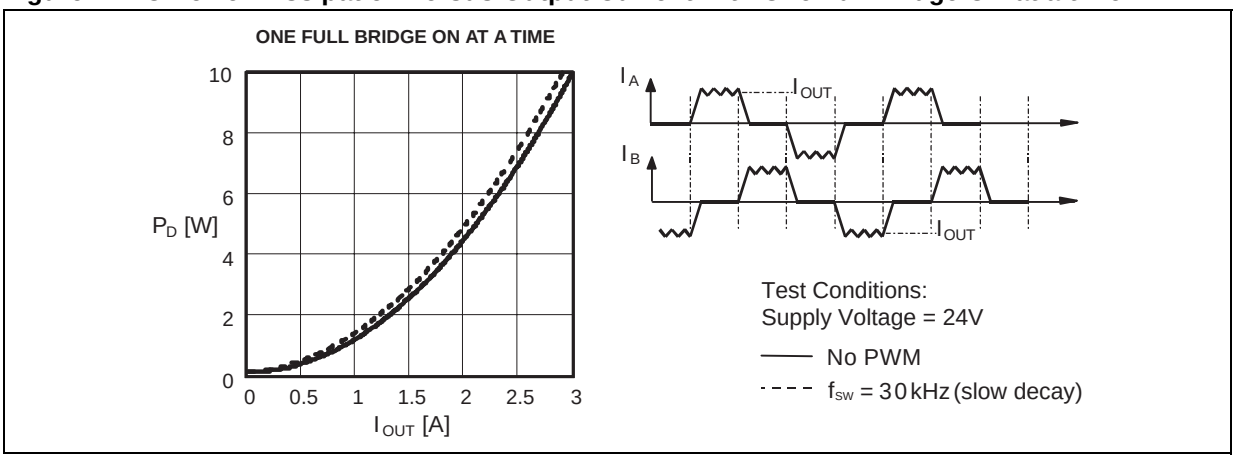
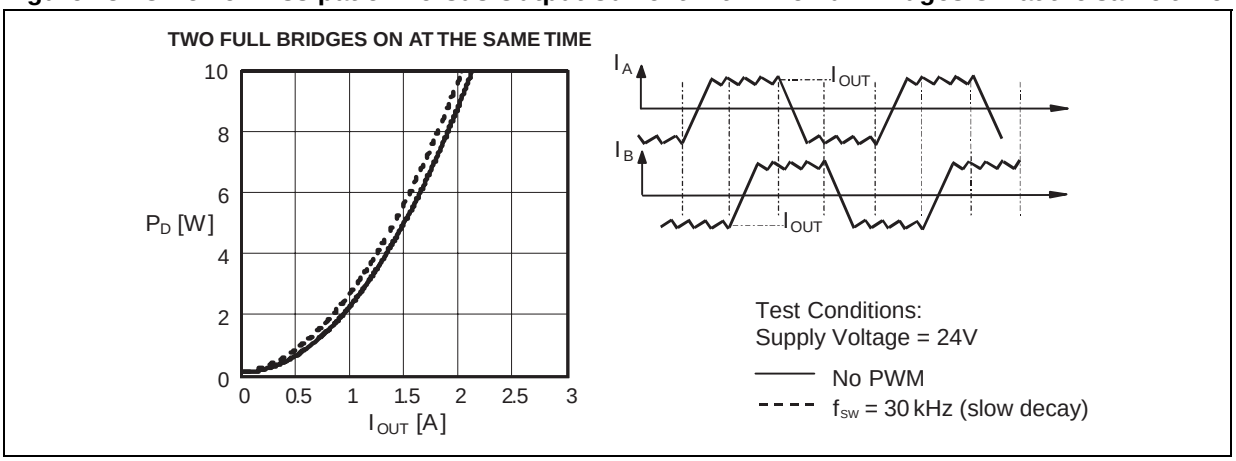


Figure 18. IC Power Dissipation versus Output Current with Two Full Bridges ON at the same time.



THERMAL MANAGEMENT

In most applications the power dissipation in the IC is the main factor that sets the maximum current that can be delivered by the device in a safe operating condition. Therefore, it has to be taken into account very carefully. Besides the available space on the PCB, the right package should be chosen considering the power dissipation. Heat sinking can be achieved using copper on the PCB with proper area and thickness. Figures 20, 21 and 22 show the Junction-to-Ambient Thermal Resistance values for the PowerSO36, PowerDIP24 and SO24 packages.

For instance, using a PowerSO package with copper slug soldered on a 1.5 mm copper thickness FR4 board with 6cm^2 dissipating footprint (copper thickness of 35µm), the $R_{th\ j\text{-}amb}$ is about 35°C/W. Fig. 19 shows mounting methods for this package. Using a multi-layer board with vias to a ground plane, thermal impedance can be reduced down to 15°C/W.

Figure 19. Mounting the PowerSO package.

Slug soldered to PCB with dissipating area

Slug soldered to PCB with dissipating area plus ground layer

Slug soldered to PCB with dissipating area plus ground layer contacted through via holes

Figure 20. PowerSO36 Junction-Ambient thermal resistance versus on-board copper area.

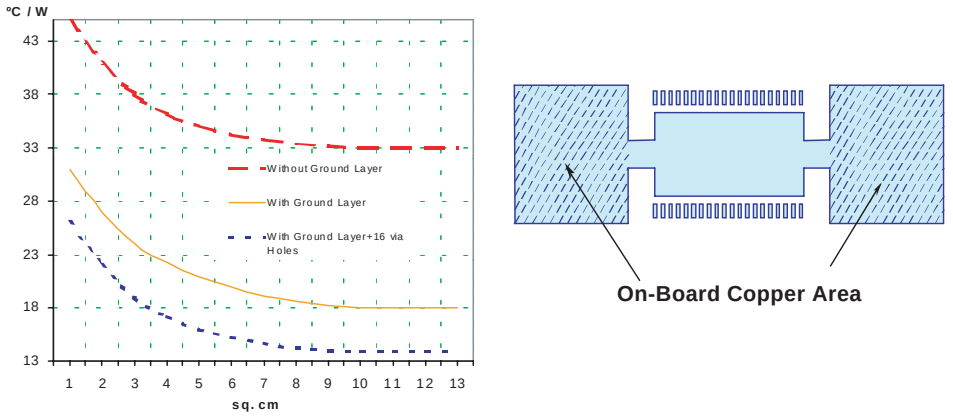


Figure 21. PowerDIP24 Junction-Ambient thermal resistance versus on-board copper area.

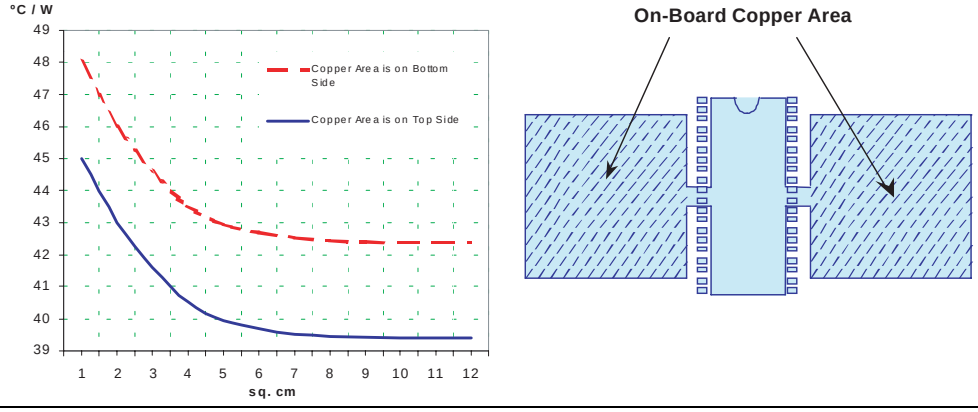


Figure 22. SO24 Junction-Ambient thermal resistance versus on-board copper area.

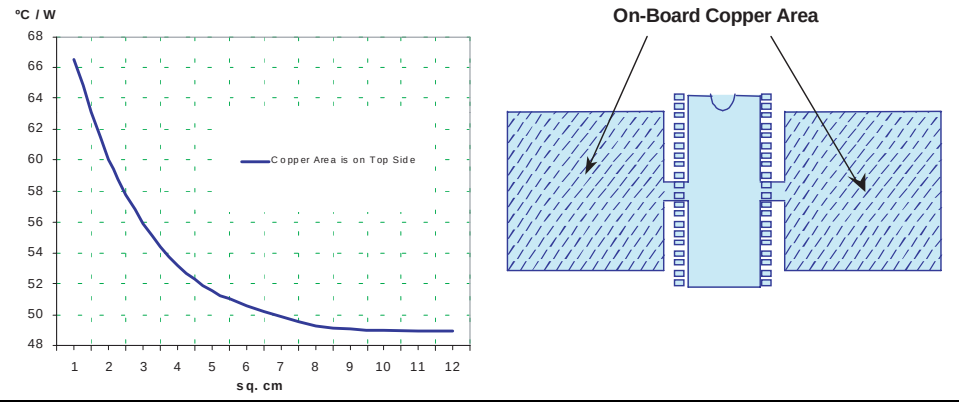


Figure 23. Typical Quiescent Current vs. Supply Voltage

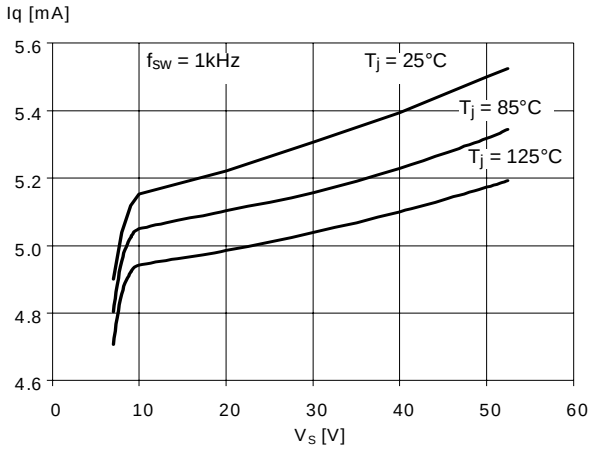


Figure 24. Normalized Typical Quiescent Current vs. Switching Frequency

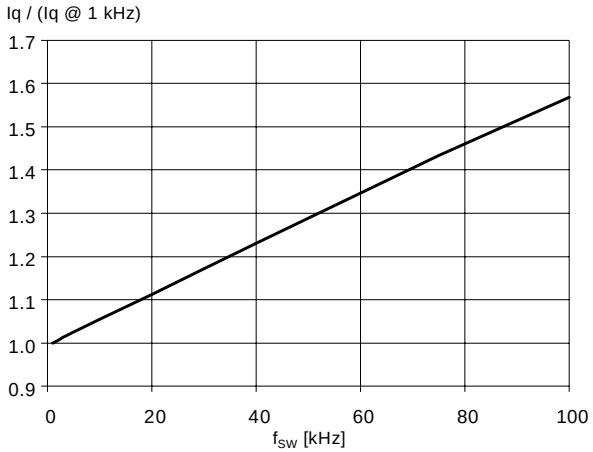


Figure 25. Typical Low-Side $R_{DS(ON)}$ vs. Supply Voltage

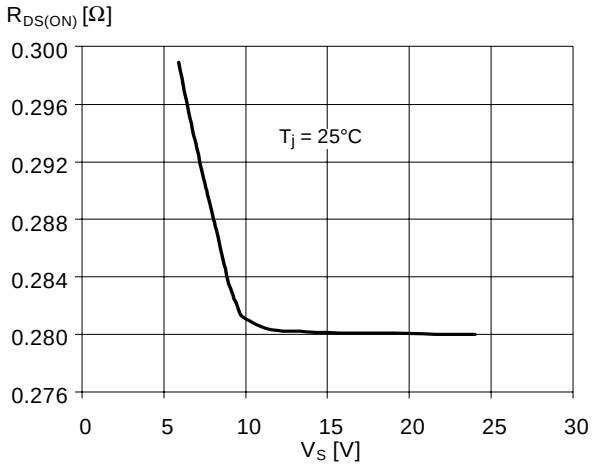


Figure 26. Typical High-Side RDS(ON) vs. Supply Voltage

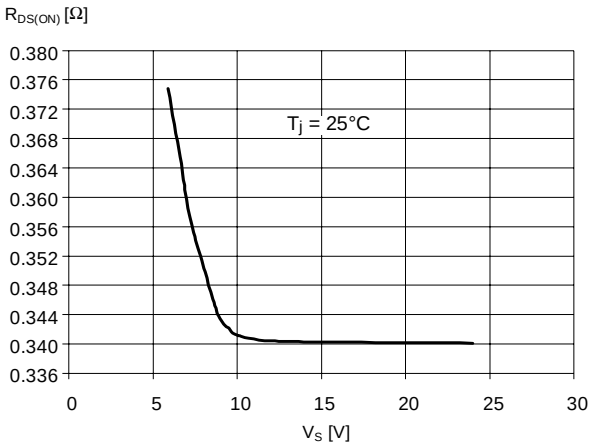


Figure 27. Normalized $R_{DS(ON)}$ vs.Junction Temperature (typical value)

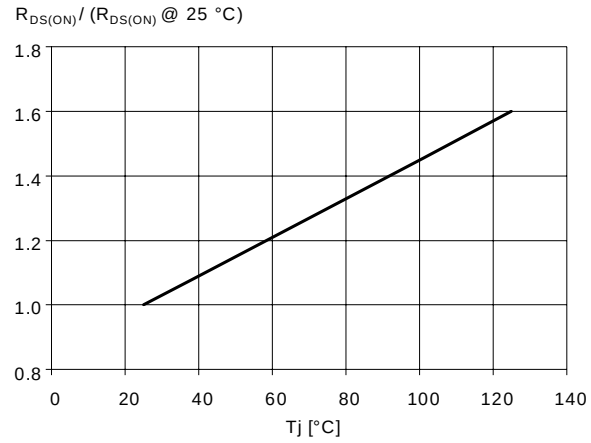
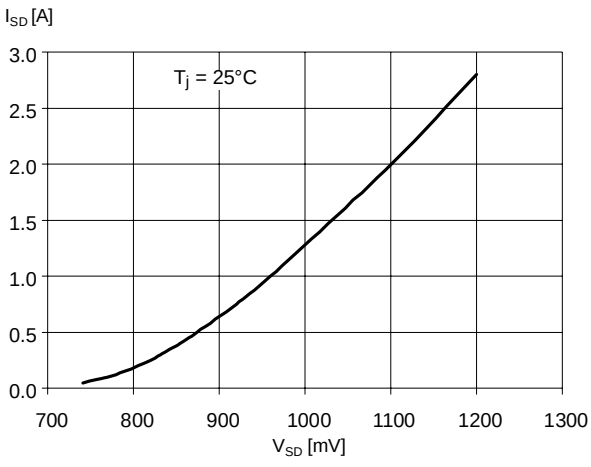


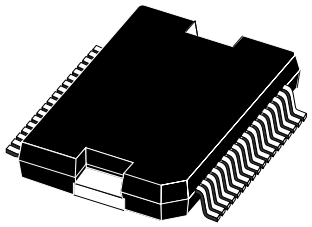
Figure 28. Typical Drain-Source Diode Forward ON Characteristic



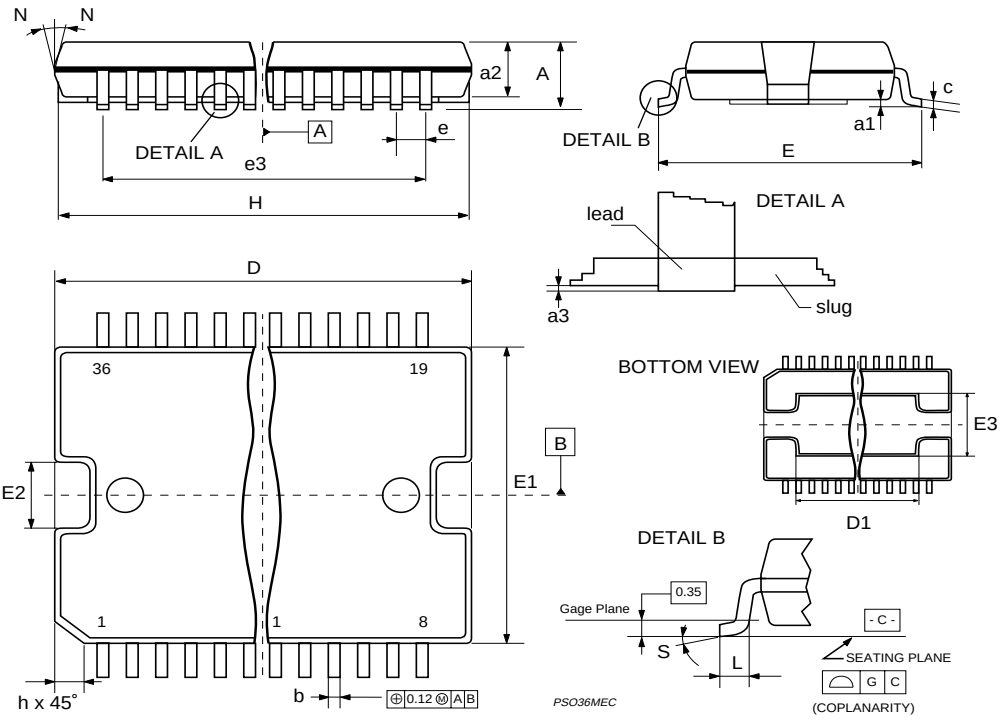
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.60			0.141
a1	0.10		0.30	0.004		0.012
a2			3.30			0.130
a3	0		0.10	0		0.004
b	0.22		0.38	0.008		0.015
c	0.23		0.32	0.009		0.012
D (1)	15.80		16.00	0.622		0.630
D1	9.40		9.80	0.370		0.385
E	13.90		14.50	0.547		0.570
e		0.65			0.0256	
e3		11.05			0.435	
E1 (1)	10.90		11.10	0.429		0.437
E2			2.90			0.114
E3	5.80		6.20	0.228		0.244
E4	2.90		3.20	0.114		0.126
G	0		0.10	0		0.004
H	15.50		15.90	0.610		0.626
h			1.10			0.043
L	0.80		1.10	0.031		0.043
N	10°(max.)					
S	8 °(max.)					

(1): "D" and "E1" do not include mold flash or protrusions
- Mold flash or protrusions shall not exceed 0.15mm (0.006 inch)
- Critical dimensions are "a3", "E" and "G".

OUTLINE AND MECHANICAL DATA

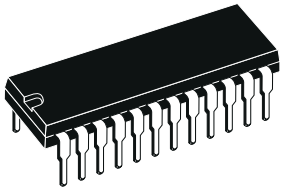


PowerSO36

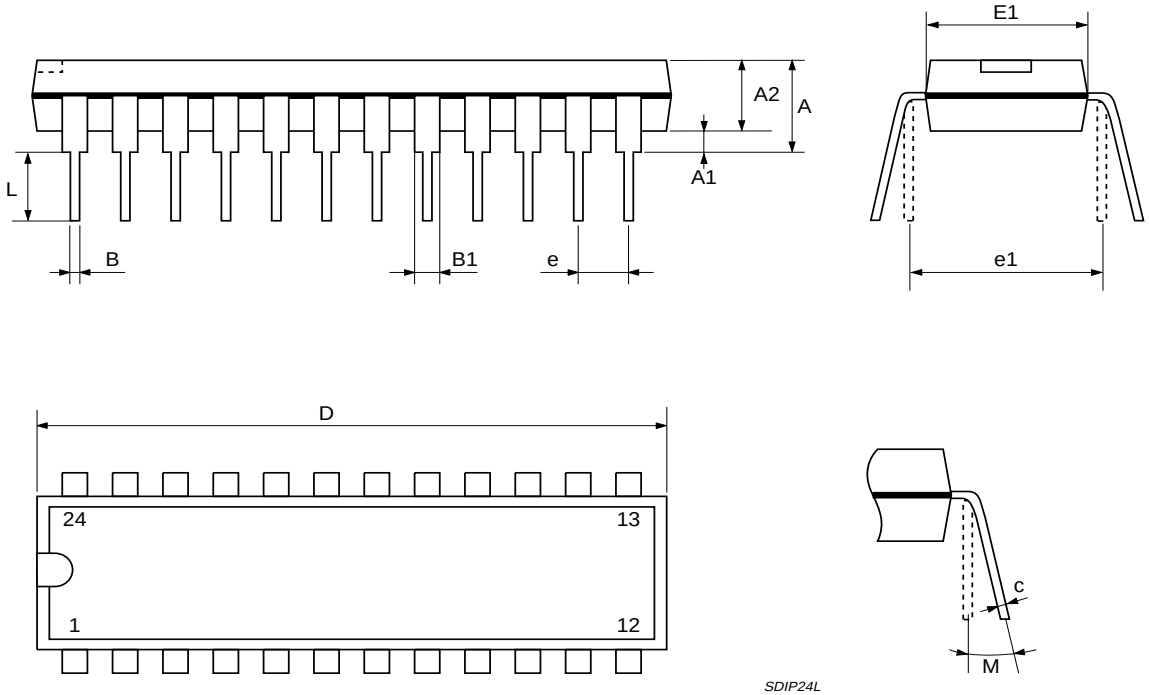


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.320			0.170
A1	0.380			0.015		
A2		3.300			0.130	
B	0.410	0.460	0.510	0.016	0.018	0.020
B1	1.400	1.520	1.650	0.055	0.060	0.065
c	0.200	0.250	0.300	0.008	0.010	0.012
D	31.62	31.75	31.88	1.245	1.250	1.255
E	7.620		8.260	0.300		0.325
e		2.54			0.100	
E1	6.350	6.600	6.860	0.250	0.260	0.270
e1		7.620			0.300	
L	3.180		3.430	0.125		0.135
M	0° min, 15° max.					

OUTLINE AND MECHANICAL DATA



Powerdip 24

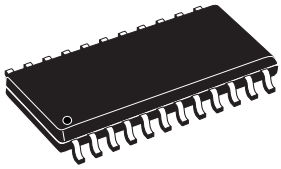


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.10		0.30	0.004		0.012
B	0.33		0.51	0.013		0.200
C	0.23		0.32	0.009		0.013
D (1)	15.20		15.60	0.598		0.614
E	7.40		7.60	0.291		0.299
e		1.27			0.050	
H	10.0		10.65	0.394		0.419
h	0.25		0;75	0.010		0.030
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

(1) "D" dimension does not include mold flash, protusions or gate burrs. Mold flash, protusions or gate burrs shall not exceed 0.15mm per side.

OUTLINE AND MECHANICAL DATA

Weight: 0.60gr



SO24